DAC-86

COMDAC® COMPANDING
D/A CONVERTER (μ-255 LAW)

Precision Monolithics Inc.

FEATURES

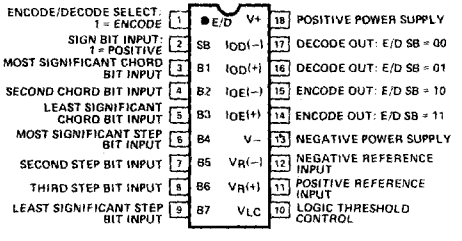
- **Conforms With Bell System μ-255 Companding Law**
- **Meets D3 Compandor Tracking Specifications**
- **Both Encode and Decode Capability**
- **Tight Full-Scale Tolerance Eliminates Calibration**
- **Low Full-Scale Drift Over Temperature**
- **Extremely Low Noise Contribution**
- **Multiplying Reference Inputs**
- **Simplifies PCM System Design**
- **High Reliability**
- **Low Power Consumption and Low Cost**
- **Two Grades Available**

GENERAL DESCRIPTION

The DAC-86 monolithic COMDAC® D/A Converter provides a 15 segment linear approximation to the Bell System μ-255 companding law. The law is implemented by using three bits to select one of eight binarily-related chords (or segments) and four bits to select one of sixteen linearly-related steps within each chord. A sign bit determines signal polarity, and an encode/decode input determines the mode of operation.

Accuracy is assured by specifying chord end point values, step nonlinearity, and monotonicity over the full operating temperature range. Typical applications include PCM carrier systems, digital PBX's intercom systems, and PCM recording. For CCITT "A" Law models, refer to the DAC-89 data sheet.

PIN CONNECTIONS & ORDERING INFORMATION

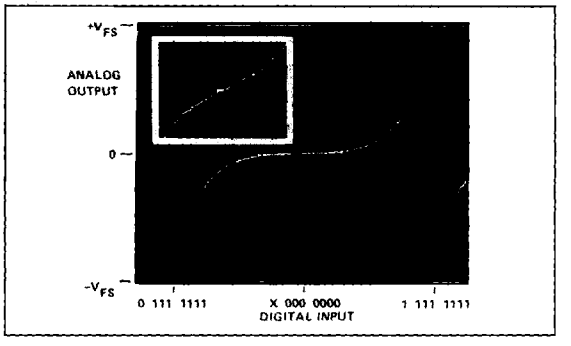


18-PIN HERMETIC DUAL-IN-LINE
(X-Suffix)

GRADE	TEMP. RANGE	ACCURACY
DAC-86EX†	−25°C/+85°C	±1/2 Step
DAC-86CX†	−25°C/+85°C	±1 Step

† Burn-in is available on commercial and industrial temperature range parts in CerDIP, plastic DIP, and TO-can packages. For ordering information, see 1990/91 Data Book, Section 2.

COMDAC® TRANSFER CHARACTERISTIC



BELL μ-255 LAW TRANSFER CHARACTERISTIC

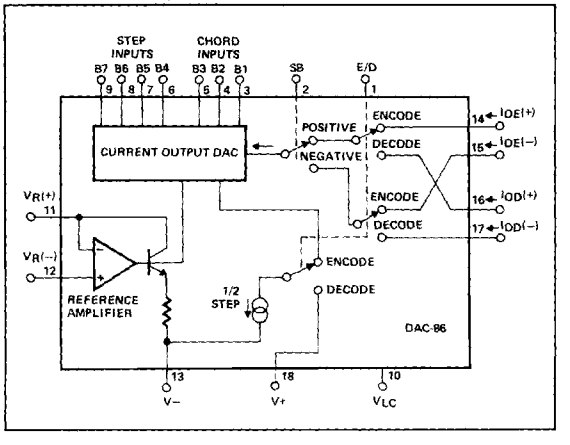
The DAC-86 transfer characteristic is a piecewise linear approximation to the Bell System μ-255 law expressed by:

$$Y(\chi) = \mathrm{sgn}(\chi)\,\frac{\ln(1+\mu|\chi|)}{\ln(1+\mu)} \quad -1 \le \chi \le 1$$

for a normalized coding range of ±1
where: χ = input signal level
Y = output compressed signal level
$\mu = 255$

This law is implemented with a eight chord (or segment) piecewise linear approximation with 16 linear steps in each chord. Dynamic range of 72dB in both polarities is achieved with eight-bit coding.

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

V+ Supply to V− Supply 36V
V_{LC} Swing ..... V− plus 8V to V+
Analog Current Outputs ..... V− plus 8V to V− plus 36V
Reference Inputs ..... V− to V+
Reference Input Differential Voltage ..... ±18V
Reference Input Current 1.25mA
Logic Inputs ..... V− plus 8V to V− plus 36V
Operating Temperature ..... −25°C to +85°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
18-Pin Hermetic DIP (X)	79	11	°C/W

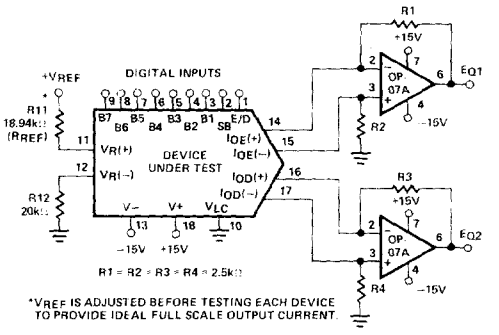
NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP package.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $I_{REF} = 528\mu A$, $-25°C \le T_A \le +85°C$, for all 4 outputs, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	DAC-86E MIN	DAC-86E TYP	DAC-86E MAX	DAC-86C MIN	DAC-86C TYP	DAC-86C MAX	UNITS
Resolution		8 chords with 16 steps each	±128	±128	±128	±128	±128	±128	Steps
Dynamic Range		20 log ($I_{7,15}/I_{0,1}$)	72	72	72	72	72	72	dB
Monotonicity		Sign-Bit + or −	128	—	—	128	—	—	Steps
Chord End-Point Accuracy All Chords		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	—	—	±1/2	—	—	±1	Step
Encode Decision Level Current		Additional output encode/decode = 1	3/8	1/2	5/8	1/4	1/2	3/4	Step
Settling Time (Note 1)	t_S	To within ±1/2 step	—	1	—	—	1	—	μsec
Full-Scale Drift (C_7) (Note 2)	ΔI_{FS}	Full temperature range	—	±1/16	±1/10	—	±1/10	±1/4	Step
Output Voltage Compliance	V_{OC}	Full-scale current change ≤ 1/2 step	−5	—	+18	−5	—	+18	Volts
Full-Scale Symmetry Error	$I_{O(+)} - I_{O(-)}$	Decode or encode pair Input Code 111 1111	—	±1/40	±1/8	—	±1/40	±1/4	Step
Zero-Scale Current (C_0)	I_{ZS}	Measured at selected output with 000 0000 input	—	±1/40	±1/8	—	±1/40	±1/4	Step
Disable Current (All bits high)	I_{DIS}	Leakage of output disabled by E/D and SB	—	5	75	—	5	75	nA
Step Accuracy All Chords		Error relative to ideal values at $I_{FS} = 2007.75\mu A$	—	—	±1/2	—	—	±1	Step
Output Current Range	I_{FSR}		—	2.0	4.2	—	2.0	4.2	mA
Logic Input Levels, Logic "0"	V_{IL}	$V_{LC} = 0V$	—	—	0.8	—	—	0.8	Volts
Logic Input Levels, Logic "1"	V_{IH}	$V_{LC} = 0V$	2	—	—	2	—	—	Volts
Logic Input Current	I_{IN}	$V_{IN} = -5V$ to $+18V$	—	—	120	—	—	120	μA
Logic Input Swing	V_{IS}	V− = −15V	−5	—	+18	−5	—	+18	Volts
Reference Bias Current	I_{12}		—	−3	−12	—	−3	−12	μA
Reference Input Slew Rate	dI/dt		—	0.25	—	—	0.25	—	mA/μs
Power Supply Sensitivity Over Supply Range (Refer to Characteristic Curves)	$PSSI_{FS+}$ $PSSI_{FS-}$	V+ = 4.5V to 18V, V− = −15V V− = −10.8V to −18V, V+ = 15V	— —	±1/20 ±1/10	±1/2 ±1/2	— —	±1/20 ±1/10	±1/2 ±1/2	Step
Power Supply Current	I+ I− I+ I−	$V_S = +5V, -15V, I_{FS} = 2.0mA$ $V_S = +5V, -15V, I_{FS} = 2.0mA$ $V_S = \pm 15V, I_{FS} = 2.0mA$ $V_S = \pm 15V, I_{FS} = 2.0mA$	— — — —	2.7 −6.7 2.7 −6.7	4.5 −9.3 4.5 −9.3	— — — —	2.7 −6.7 2.7 −6.7	4.5 −9.3 4.5 −9.3	mA
Power Dissipation	P_d	$V_S = +5V, -15V, I_{FS} = 2.0mA$ $V_S = \pm 15V, I_{FS} = 2.0mA$	— —	114 141	167 207	— —	114 141	167 207	mW

NOTE:
1. In a companding DAC the term LSB is not used because the step size within each chord is different. For example, in the first chord around zero (C_0) step size is 0.5μA, while in the last chord near full-scale (C_7) step size is 64μA. Settling time varies for each of the chord bits and step bits and a maximum specification is misleading. In decode operation, the DAC-86 and OP-16 combination will decode eight channels. In the encode mode, the DAC-86 and CMP-01 combination will encode eight channels. Both encode and decode statements assume a 5.2μsec channel time.
2. Guaranteed by design.

OUTPUT CURRENT DC TEST CIRCUIT



LINE SELECTION TABLE

TEST GROUP	ENCODE/ DECODE	SIGN BIT	OUTPUT MEASUREMENT	
1	1	1	$I_{OE}(+)$	$(E_{O1}/R1)$
2	1	0	$I_{OE}(-)$	$(E_{O1}/R2)$
3	0	1	$I_{OD}(+)$	$(E_{O2}/R3)$
4	0	0	$I_{OD}(-)$	$(E_{O2}/R4)$

NOTE: Accuracy is specified in the test circuit using the tables below to be within the specified proportion of a step at the maximum value in each chord. Monotonicity is guaranteed for all input codes.

CONDENSED CURRENT OUTPUT TABLES (I_{REF} = 528μA)

IDEAL DECODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

STEP \ CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.0	8.25	24.75	57.75	123.75	255.75	519.75	1047.75
15	1111	7.5	23.25	54.75	117.75	243.75	495.75	999.75	2007.75
STEP SIZE		0.5	1	2	4	8	16	32	64

IDEAL ENCODE OUTPUT CURRENT IN MICROAMPS AT CHORD ENDPOINTS

STEP \ CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	0.25	8.75	25.75	59.75	127.75	263.75	535.75	1079.75
15	1111	7.75	23.25	55.75	119.75	247.75	503.75	1015.75	2039.75
STEP SIZE		0.50	1	2	4	8	16	32	64

NOTE:
These tables may be extended to include all of the encode/decode currents (ideal with SI_{REF} = 528μA) by multiplying any of the numbers in the normalized tables by 0.5μA.

PARAMETER DEFINITIONS

FULL-SCALE DRIFT
The change in output current over the full operating temperature with V_{REF} = 10.000V, R11 = 18.94kΩ, and R12 = 20kΩ.

FULL-SCALE SYMMETRY ERROR
The difference between $I_{OD}(-)$ and $I_{OD}(+)$ or the difference between $I_{OE}(-)$ and $I_{OE}(+)$ at full-scale output.

OUTPUT VOLTAGE COMPLIANCE
The maximum output voltage swing at any current level which causes < 1/2 step change in output current.

CHORDS
Groups of linearly-related steps in the transfer function. Also known as segments.

CHORD ENDPOINTS
The maximum code in each chord; used to specify accuracy.

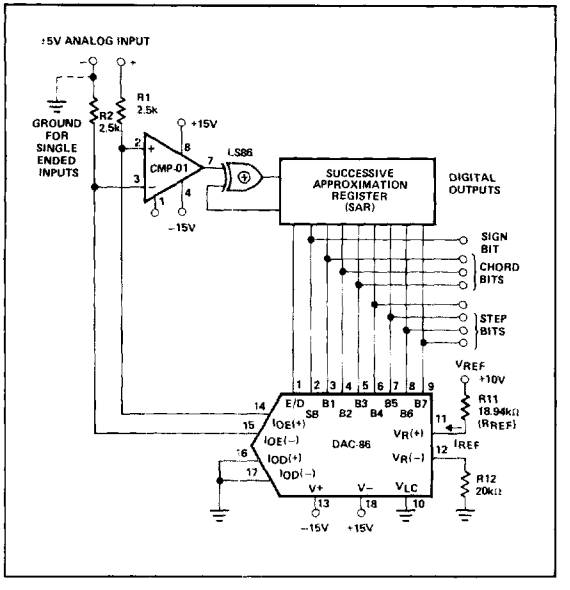
STEPS
Increments in each chord which divides the chord into 16 equal levels.

OUTPUT LEVEL NOTATION
Each output current level may be designated by the code $I_{C,S}$ where C = chord number and S = step number. For example, $I_{0,0}$ = zero-scale current; $I_{0,1}$ = first step from zero; $I_{0,15}$ = endpoint of first chord (C_0); $I_{7,15}$ = full-scale current.

DYNAMIC RANGE
Ratio of full-scale current to step size in chord zero, expressed in dB. This can be measured peak or peak-to-peak with the same result.

BASIC ENCODE OPERATION (COMPRESSING A/D CONVERSION)

BASIC ENCODE CONNECTIONS



ENCODE DECISION LEVELS

Compressing A/D conversion with the DAC-86 requires a comparator, an EXCLUSIVE-OR gate, and a successive approximation register — the usual elements in any sign-magnitude A/D converter. However, a compressing A/D has one significant difference. In a conventional (linear converter), the step size is a constant percentage of full-scale. In a compressing A/D converter, the step size increases as the output changes from zero-scale to full-scale.

When the DAC is used in the feedback loop of a successive approximation analog to digital converter (ADC) the DAC outputs are used as decision levels to determine the edges of the quantizing bands. When the DAC is used in the decode mode the outputs correspond to the center of the quantizing bands. The encode mode output exceeds the decode mode output by one-half step. See AN-39 for detailed explanation.

ENCODING SEQUENCE

An encoding sequence begins with the sign-bit decision. During this time the comparator functions as a polarity detector. The encode/decode (E/D) input is held at a logic "0". In this mode, current flows into the decode outputs, and the comparator is effectively disconnected from the DAC. Once the input polarity has been determined, the E/D input toggles to a logic "1" allowing current to flow into $I_{OE}(+)$ or $I_{OE}(-)$.

For positive inputs, current flows into $I_{OE}(+)$ through R1, and the comparator's output is entered as the answer for each successive decision. For negative inputs, current flows into $I_{OE}(-)$ through R2 developing a negative voltage which is compared with the analog input. An EXCLUSIVE-OR gate inverts the comparator's output during negative trials to maintain the proper logic coding, all ones for full-scale and all zeros for zero-scale.

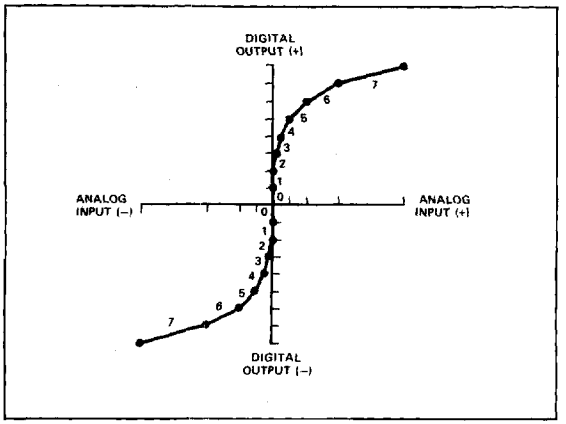
The bits are converted with a successive removal technique, starting with a decision at the code 011 1111 and turning off bits sequentially until all decisions have been made.

NORMALIZED ENCODE LEVEL (SIGN BIT EXCLUDED) $(I_{C,S} = 2[2^C (S + 17) - 16.5]$

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP \ CHORD		0	1	2	3	4	5	6	7
STEP		000	001	010	011	100	101	110	111
0	0000	1	35	103	239	511	1055	2143	4319
1	0001	3	39	111	255	543	1119	2271	4575
2	0010	5	43	119	271	575	1183	2399	4831
3	0011	7	47	127	287	607	1247	2527	5087
4	0100	9	51	135	303	639	1311	2655	5343
5	0101	11	55	143	319	671	1375	2783	5599
6	0110	13	59	151	335	703	1439	2911	5855
7	0111	15	63	159	351	735	1503	3039	6111
8	1000	17	67	167	367	767	1567	3167	6367
9	1001	19	71	175	383	799	1631	3295	6623
10	1010	21	75	183	399	831	1695	3423	6879
11	1011	23	79	191	415	863	1759	3551	7135
12	1100	25	83	199	431	895	1823	3679	7391
13	1101	27	87	207	447	927	1887	3807	7647
14	1110	29	91	215	463	959	1951	3935	7903
15	1111	31	95	223	479	991	2015	4063	8159
STEP SIZE		2	4	8	16	32	64	128	256

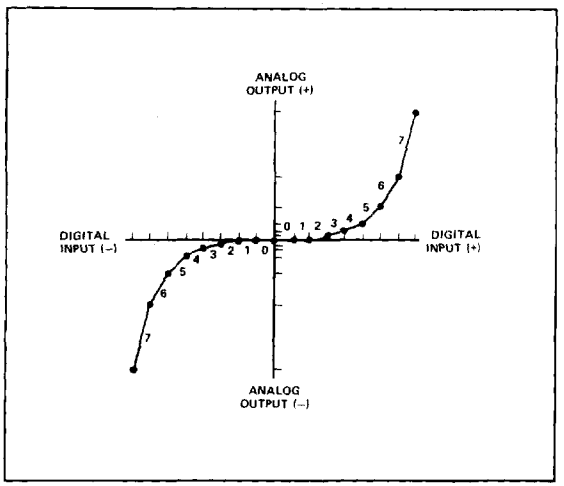
ENCODE TRANSFER CHARACTERISTICS (A/D CONVERSION)



BASIC DECODE OPERATION (EXPANDING D/A CONVERSION)

D/A conversion with the DAC-86 is implemented by using an operational amplifier connected to the decode outputs. The decode mode of operation is selected by applying a logic "0" to the encode/decode input. This enables the $I_{OD}(+)$ or $I_{OD}(-)$ to be selected by the sign-bit input. When the sign-bit input is high, a logic "1", all of the output current flows into $I_{OD}(+)$ forcing a positive voltage at the operational amplifier's output. When the sign-bit input is low, logic "0", all of the output current flows into $I_{OD}(-)$ through R2 forcing a negative voltage output. The sign-bit steers current into $I_{OD}(+)$ or $I_{OD}(-)$, therefore the output will always be symmetrical, limited only by the matching of R1 and R2.

DECODE TRANSFER CHARACTERISTIC (D/A CONVERSION)



NORMALIZED DECODE OUTPUT (SIGN BIT EXCLUDED) ($I_{C,S}=2[2^C(S+16.5)-16.5]$)

C = chord no. (0 through 7)
S = step no. (0 through 15)

STEP \ CHORD		0	1	2	3	4	5	6	7
		000	001	010	011	100	101	110	111
0	0000	0	33	99	231	495	1023	2079	4191
1	0001	2	37	107	247	527	1087	2207	4447
2	0010	4	41	115	263	559	1151	2335	4703
3	0011	6	45	123	279	591	1215	2463	4959
4	0100	8	49	131	295	623	1279	2591	5215
5	0101	10	53	139	311	655	1343	2719	5471
6	0110	12	57	147	327	687	1407	2847	5727
7	0111	14	61	155	343	719	1471	2975	5983
8	1000	16	65	163	359	751	1535	3103	6239
9	1001	18	69	171	375	783	1599	3231	6495
10	1010	20	73	179	391	815	1663	3359	6751
11	1011	22	77	187	407	847	1727	3487	7007
12	1100	24	81	195	423	879	1791	3615	7263
13	1101	26	85	203	439	911	1855	3743	7519
14	1110	28	89	211	455	943	1919	3871	7775
15	1111	30	93	219	471	975	1983	3999	8031
STEP SIZE		2	4	8	16	32	64	128	256

NORMALIZED TABLES

The encode and decode tables are used to calculate the ideal output current at any point. For example, in decode mode at $I_{3,7}$ (011 0111) find 343. 343/8031 × I_{FS} = 85.75μA (I_{FS} = 2007.75μA). Alternatively, use the condensed current tables and add up the number of steps.

BASIC REFERENCE CONSIDERATIONS

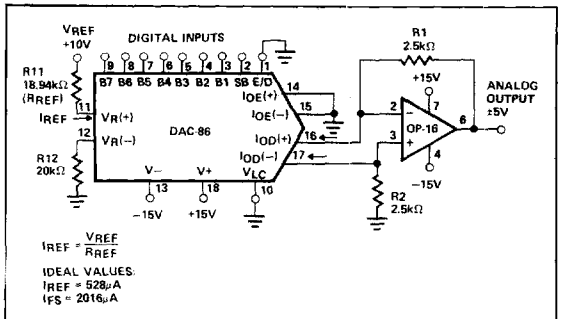
Full-scale output current is ideally 2007.75μA when the reference current is 528μA in the decode mode. In the encode mode I_{FS} = 2039.75μA due to the additional 1/2 step (32μA). A percentage change in I_{REF} will produce the same percentage change in output current.

The large step size at full-scale allows the use of inexpensive references in many applications. In some situations V_{REF} may even be the positive power supply. For example, with V+ = 15V, R_{REF} = 15V/528μA or 28.4kΩ. When using a power supply as a reference, R11 becomes two resistors, R11A and R11B, and the junction bypassed to ground with a 0.1μf monolithic capacitor.

DECODE OUTPUT VOLTAGE

	E/D	SB	B1	B2	B3	B4	B5	B6	B7	VOLT
POS FULL-SCALE	0	1	1	1	1	1	1	1	1	5.019V
(+) ZERO-SCALE +1 STEP	0	1	0	0	0	0	0	0	1	0.0012
(+) ZERO-SCALE	0	1	0	0	0	0	0	0	0	0V
(−) ZERO-SCALE	0	0	0	0	0	0	0	0	0	0V
(−) ZERO-SCALE +1 STEP	0	0	0	0	0	0	0	0	1	-0.0012
NEG FULL-SCALE	0	0	1	1	1	1	1	1	1	-5.019V

BASIC DECODE CONNECTIONS



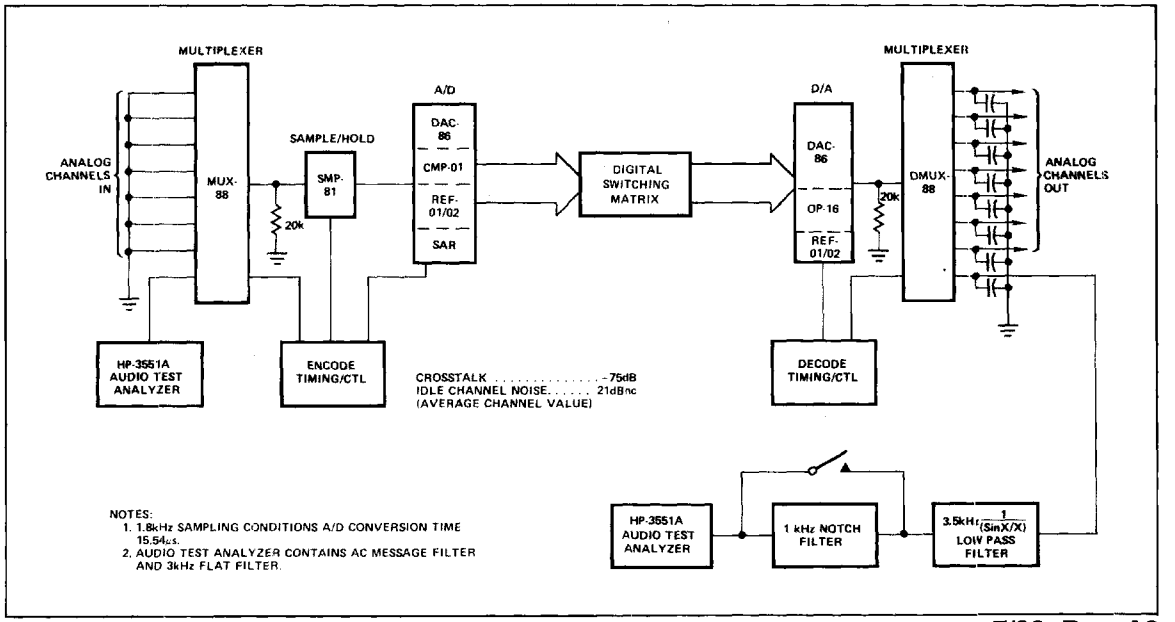
NOTE: THIS CONFIGURATION WILL DECODE 24 CHANNELS.

REFERENCE AMPLIFIER SETUP

The DAC-86 is a multiplying D/A converter. The output current is the product of the normalized digital input and the input reference current. The reference current may be fixed or may vary from nearly zero to +1.0mA. The full-scale output current is a linear function of the reference current.

In external reference applications a positive reference voltage forces current through R11 in the the $V_R(+)$ terminal (pin 11) of the reference amplifier. Alternatively, a negative reference may be applied to $V_R(-)$ at pin 12; reference current flows from ground through R11 into $V_R(+)$. This negative reference connection has the advantage of presenting a very high impedance at pin 12. The voltage at pin 11 is equal to and tracks the voltage at pin 12 due to the high gain of the internal

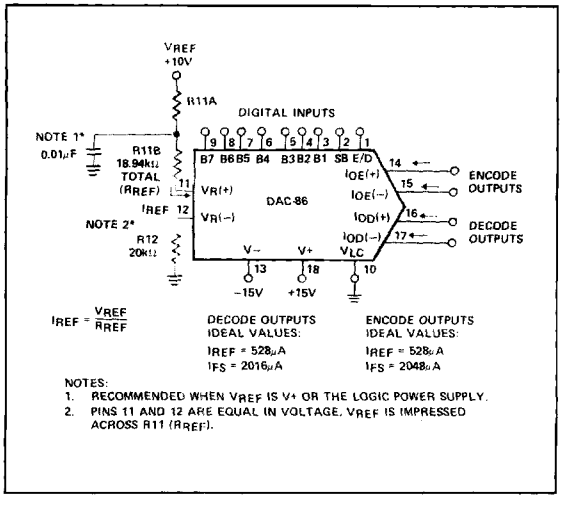
SYSTEM TEST CIRCUIT



NOTES:
1. 1.8kHz SAMPLING CONDITIONS A/D CONVERSION TIME 15.54μs.
2. AUDIO TEST ANALYZER CONTAINS AC MESSAGE FILTER AND 3kHz FLAT FILTER.

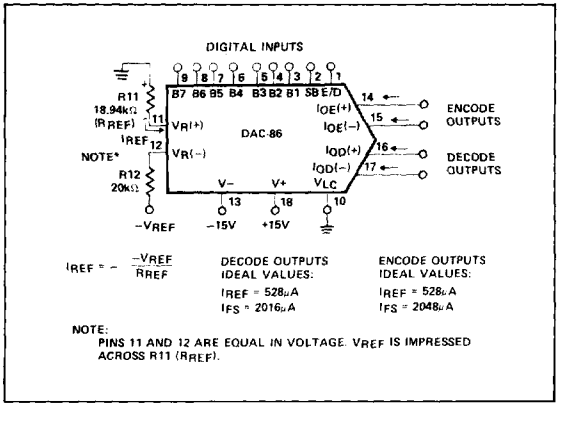
reference amplifier. R12 (nominally equal to R11) is used to cancel bias current errors and may be eliminated with a minor increase in error.

POSITIVE REFERENCE OPERATION



NOTES:
1. RECOMMENDED WHEN V_{REF} IS V+ OR THE LOGIC POWER SUPPLY.
2. PINS 11 AND 12 ARE EQUAL IN VOLTAGE. V_{REF} IS IMPRESSED ACROSS R11 (R_{REF}).

NEGATIVE REFERENCE OPERATION



NOTE:
PINS 11 AND 12 ARE EQUAL IN VOLTAGE. V_{REF} IS IMPRESSED ACROSS R11 (R_{REF}).

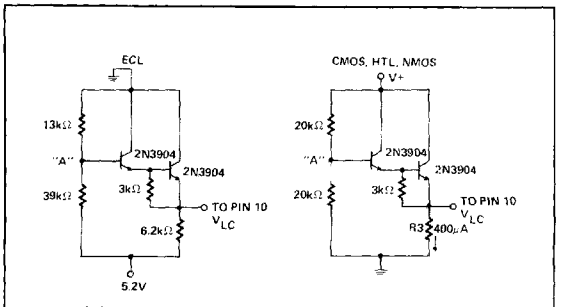
REFERENCE AMPLIFIER OPERATION

For most applications a +10.0V reference, such as the PMI REF-01, is recommended for optimum full-scale temperature performance. (This also minimizes the contributions of reference amplifier V_{OS} and TCV_{OS}). For most applications the tight relationship between I_{REF} and I_{FS} eliminates the need for trimming I_{REF}; but if desired full-scale trimming is accomplished by selecting R11 or by using a potentiometer for R11.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common-mode range. While the recommended operating range of DC reference current is 0.1mA to 1.0mA, monotonic operation is maintained over an even wider range.

LOGIC INPUT AND POWER SUPPLY CONSIDERATIONS

INTERFACING CIRCUIT FOR ECL, CMOS, HTL, AND NMOS LOGIC INPUTS



NOTES:
1. SET THE VOLTAGE "A" TO BE AT THE DESIRED LOGIC INPUT SWITCHING THRESHOLD.
2. ALLOWABLE RANGE OF LOGIC THRESHOLD IS TYPICALLY −5V TO +13V WHEN OPERATING THE DAC-86 ON ±15V SUPPLIES.

LOGIC INPUTS

The DAC-86 interfaces with various logic families by referencing V_{LC} (pin 10) at a potential which is 1.4V below the desired logic input switching threshold. However, this voltage source must be capable of sourcing and sinking a changing current at pin 10.

The negative voltage at the logic inputs must be limited to +10V with respect to V− (pin 13).

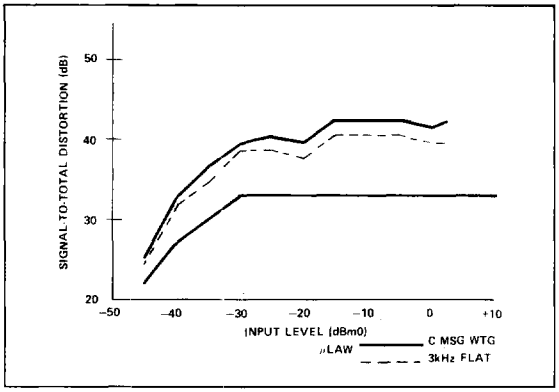
POWER SUPPLIES

Power supply current drain is relatively independent of voltage and temperature and completely independent of the logic input states.

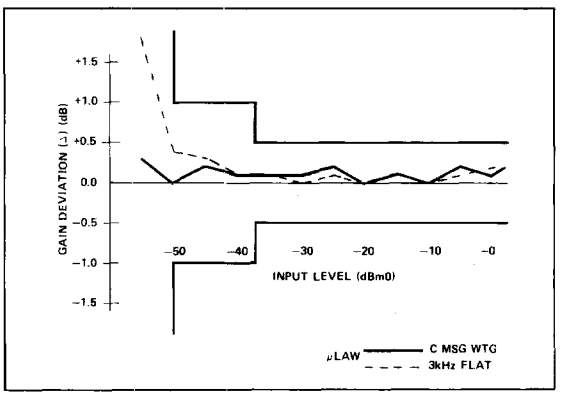
When operating with V− between −15V and −11V, output negative voltage compliance, $V_{OC}(-)$, reference input amplifier common-mode voltage range, and logic input negative voltage range are reduced by an amount equivalent to the difference between −15V and the V− supply in use. Operation with V+ between +5V and +15V affects V_{LC} and the reference amplifier common-mode positive voltage range in the same manner.

SYSTEM PERFORMANCE CHARACTERISTICS

SIGNAL TO QUANTIZING DISTORTION vs INPUT LEVEL



GAIN TRACKING



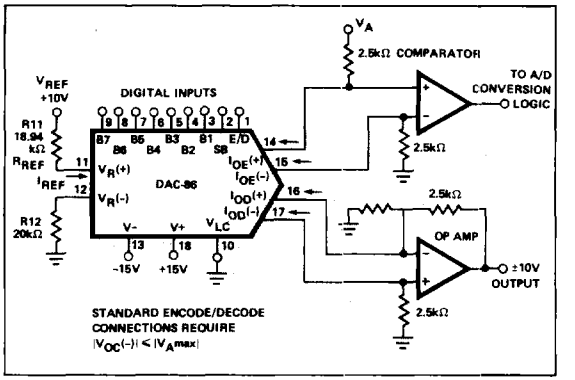
OUTPUT VOLTAGE COMPLIANCE

The DAC-86 has true current outputs with wide voltage compliance that enables single ended and balanced load drive capability. Positive voltage compliance is +18V and negative voltage compliance is −5.0V with I_{REF} = 528μA and V = −15V. Negative voltage compliance $V_{OC}(-)$ for other values of I_{REF} and V− may be obtained from the table, or calculated as follows:

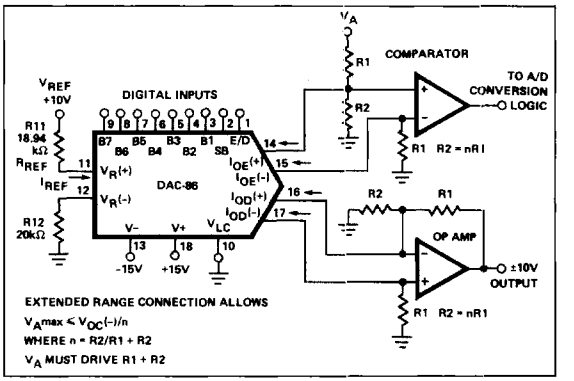
$$V_{OC}(-)\ \text{min} = (V-) + (2\ I_{REF} \times 1.6k\Omega) + 8.4V$$

Output voltage compliance can be extended in both encode and decode modes using the connections shown above.

STANDARD OUTPUT CONNECTIONS



OUTPUT COMPLIANCE EXTENSION CONNECTIONS



NEGATIVE OUTPUT VOLTAGE COMPLIANCE $V_{OC}(-)$

	I_{FS}		
V−	1.0mA	2.0mA	4.0mA
−12V	−2.8V	−2.0V	−0.4V
−15V	−5.8V	−5.0V	−3.4V
−18V	−8.8V	−8.0V	−6.4V

MINIMUM NEGATIVE COMPLIANCE

$V_{OC}(-)\ \text{MIN} = (V-) + (2\ I_{REF}\ 1.6k\Omega) + 8.4V$

DICE

For applicable DICE information, see DAC-88 Data Sheet.