# CA3096, CA3096A, CA3096C

NPN/PNP Transistor Arrays

FN595
Rev.5.00
January 2004

## Applications

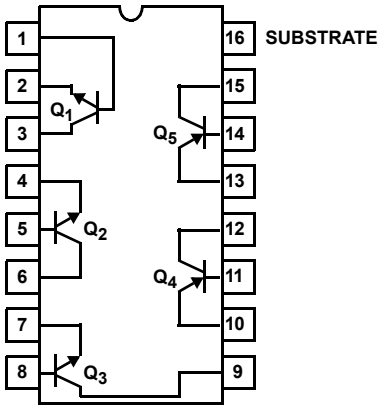
- **Five-Independent Transistors**
  - **Three NPN and**
  - **Two PNP**
- **Differential Amplifiers**
- **DC Amplifiers**
- **Sense Amplifiers**
- **Level Shifters**
- **Timers**
- **Lamp and Relay Drivers**
- **Thyristor Firing Circuits**
- **Temperature Compensated Amplifiers**
- **Operational Amplifiers**

## Part Number Information

| PART NUMBER (BRAND) | TEMP. RANGE ($^oC$) | PACKAGE | PKG. NO. |
|---|---|---|---|
| CA3096AE | -55 to 125 | 16 Ld PDIP | E16.3 |
| CA3096AM (3096A) | -55 to 125 | 16 Ld SOIC | M16.15 |
| CA3096AM96 (3096A) | -55 to 125 | 16 Ld SOIC Tape and Reel | M16.15 |
| CA3096CE | -55 to 125 | 16 Ld PDIP | E16.3 |
| CA3096E | -55 to 125 | 16 Ld PDIP | E16.3 |
| CA3096M (3096) | -55 to 125 | 16 Ld SOIC | M16.15 |
| CA3096M96 (3096) | -55 to 125 | 16 Ld SOIC Tape and Reel | M16.15 |

## Pinout

**CA3096, CA3096A, CA3096C**
**(PDIP, SOIC)**
TOP VIEW




## Description

The CA3096C, CA3096, and CA3096A are general purpose high voltage silicon transistor arrays. Each array consists of five independent transistors (two PNP and three NPN types) on a common substrate, which has a separate connection. Independent connections for each transistor permit maximum flexibility in circuit design.

Types CA3096A, CA3096, and CA3096C are identical, except that the CA3096A specifications include parameter matching and greater stringency in $I_{CBO}$, $I_{CEO}$, and $V_{CE}$(SAT). The CA3096C is a relaxed version of the CA3096.

## CA3096, CA3096A, CA3096C Essential Differences

| CHARACTERISTIC | | CA3096A | CA3096 | CA3096C |
|---|---|---|---|---|
| $V_{(BR)CEO}$ (V) (Min) | | | | |
| | NPN | 35 | 35 | 24 |
| | PNP | -40 | -40 | -24 |
| $V_{(BR)CBO}$ (V) (Min) | | | | |
| | NPN | 45 | 45 | 30 |
| | PNP | -40 | -40 | -24 |
| $h_{FE}$ at 1mA | | | | |
| | NPN | 150-500 | 150-500 | 100-670 |
| | PNP | 20-200 | 20-200 | 15-200 |
| $h_{FE}$ at 100µA | | | | |
| | PNP | 40-250 | 40-250 | 30-300 |
| $I_{CBO}$ (nA) (Max) | | | | |
| | NPN | 40 | 100 | 100 |
| | PNP | -40 | -100 | -100 |
| $I_{CEO}$ (nA) (Max) | | | | |
| | NPN | 100 | 1000 | 1000 |
| | PNP | -100 | -1000 | -1000 |
| $V_{CE\ SAT}$ (V) (Max) | | | | |
| | NPN | 0.5 | 0.7 | 0.7 |
| $\|V_{IO}\|$ (mV) (Max) | | | | |
| | NPN | 5 | - | - |
| | PNP | 5 | - | - |
| $\|I_{IO}\|$ (µA) (Max) | | | | |
| | NPN | 0.6 | - | - |
| | PNP | 0.25 | - | - |

## Absolute Maximum Ratings

| | NPN | PNP |
|---|---|---|
| Collector-to-Emitter Voltage, $V_{CEO}$ | | |
| CA3096, CA3096A | 35V | -40V |
| CA3096C | 24V | -24V |
| Collector-to-Base Voltage, $V_{CBO}$ | | |
| CA3096, CA3096A | 45V | -40V |
| CA3096C | 30V | -24V |
| Collector-to-Substrate Voltage, $V_{CIO}$ (Note 1) | | |
| CA3096, CA3096A | 45V | - |
| CA3096C | 30V | - |
| Emitter-to-Substrate Voltage, $V_{EIO}$ | | |
| CA3096, CA3096A | - | -40V |
| CA3096C | - | -24V |
| Emitter-to-Base Voltage, $V_{EBO}$ | | |
| CA3096, CA3096A | 6V | -40V |
| CA3096C | 6V | -24V |
| Collector Current, $I_C$ (All Types) | 50mA | -10mA |
| Temperature Range | -55°C to 125°C | |

## Operating Conditions

## Thermal Information

| Thermal Resistance (Typical, Note 2) | $\theta_{JA}$ (°C/W) |
|---|---|
| PDIP Package | 110 |
| SOIC Package | 120 |
| Maximum Power Dissipation (Each Transistor, Note 3) | 200mW |
| Maximum Junction Temperature (Plastic Package) | 150°C |
| Maximum Storage Temperature Range | -65°C to 150°C |
| Maximum Lead Temperature (Soldering 10s) (SOIC - Lead Tips Only) | 300°C |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTES:

1. The collector of each transistor of the CA3096 is isolated from the substrate by an integral diode. The substrate (Terminal 16) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.
2. $\theta_{JA}$ is measured with the component mounted on an evaluation PC board in free air.
3. Care must be taken to avoid exceeding the maximum junction temperature. Use the total power dissipation (all transistors) and thermal resistances to calculate the junction temperature.

## Electrical Specifications For Equipment Design, At $T_A = 25°C$

| PARAMETER | TEST CONDITIONS | CA3096 | | | CA3096A | | | CA3096C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| **DC CHARACTERISTICS FOR EACH NPN TRANSISTOR** | | | | | | | | | | | |
| $I_{CBO}$ | $V_{CB}$ = 10V, $I_E$ = 0 | - | 0.001 | 100 | - | 0.001 | 40 | - | 0.001 | 100 | nA |
| $I_{CEO}$ | $V_{CE}$ = 10V, $I_B$ = 0 | - | 0.006 | 1000 | - | 0.006 | 100 | - | 0.006 | 1000 | nA |
| $V_{(BR)CEO}$ | $I_C$ = 1mA, $I_B$ = 0 | 35 | 50 | - | 35 | 50 | - | 24 | 35 | - | V |
| $V_{(BR)CBO}$ | $I_C$ = 10μA, $I_E$ = 0 | 45 | 100 | - | 45 | 100 | - | 30 | 80 | - | V |
| $V_{(BR)CIO}$ | $I_{CI}$ = 10μA, $I_B = I_E$ = 0 | 45 | 100 | - | 45 | 100 | - | 30 | 80 | - | V |
| $V_{(BR)EBO}$ | $I_E$ = 10μA, $I_C$ = 0 | 6 | 8 | - | 6 | 8 | - | 6 | 8 | - | V |
| $V_Z$ | $I_Z$ = 10μA | 6 | 7.9 | 9.8 | 6 | 7.9 | 9.8 | 6 | 7.9 | 9.8 | V |
| $V_{CE\ SAT}$ | $I_C$ = 10mA, $I_B$ = 1mA | - | 0.24 | 0.7 | - | 0.24 | 0.5 | - | 0.24 | 0.7 | V |
| $V_{BE}$ (Note 4) | $I_C$ = 1mA, $V_{CE}$ = 5V | 0.6 | 0.69 | 0.78 | 0.6 | 0.69 | 0.78 | 0.6 | 0.69 | 0.78 | V |
| $h_{FE}$ (Note 4) | | 150 | 390 | 500 | 150 | 390 | 500 | 100 | 390 | 670 | |
| $\lvert\Delta V_{BE}/\Delta T\rvert$ (Note 4) | $I_C$ = 1mA, $V_{CE}$ = 5V | - | 1.9 | - | - | 1.9 | - | - | 1.9 | - | mV/°C |
| **DC CHARACTERISTICS FOR EACH PNP TRANSISTOR** | | | | | | | | | | | |
| $I_{CBO}$ | $V_{CB}$ = -10V, $I_E$ = 0 | - | -0.06 | -100 | - | -0.006 | -40 | - | -0.06 | -100 | nA |
| $I_{CEO}$ | $V_{CE}$ = -10V, $I_B$ = 0 | - | -0.12 | -1000 | - | -0.12 | -100 | - | -0.12 | -1000 | nA |

## Electrical Specifications For Equipment Design, At $T_A = 25^oC$ (Continued)

| PARAMETER | TEST CONDITIONS | CA3096 | | | CA3096A | | | CA3096C | | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | MIN | TYP | MAX | MIN | TYP | MAX | |
| $V_{(BR)CEO}$ | $I_C$ = -100μA, $I_B$ = 0 | -40 | -75 | - | -40 | -75 | - | -24 | -30 | - | V |
| $V_{(BR)CBO}$ | $I_C$ = -10μA, $I_E$ = 0 | -40 | -80 | - | -40 | -80 | - | -24 | -60 | - | V |
| $V_{(BR)EBO}$ | $I_E$ = -10μA, $I_C$ = 0 | -40 | -100 | - | -40 | -100 | - | -24 | -80 | - | V |
| $V_{(BR)EIO}$ | $I_{EI}$ = 10μA, $I_B = I_C$ = 0 | 40 | 100 | - | 40 | 100 | - | 24 | 80 | - | V |
| $V_{CE\ SAT}$ | $I_C$ = -1mA, $I_B$ = -100μA | - | -0.16 | -0.4 | - | -0.16 | -0.4 | - | -0.16 | -0.4 | V |
| $V_{BE}$ (Note 4) | $I_C$ = -100μA, $V_{CE}$ = -5V | -0.5 | -0.6 | -0.7 | -0.5 | -0.6 | -0.7 | -0.5 | -0.6 | -0.7 | V |
| $h_{FE}$ (Note 4) | $I_C$ = -100μA, $V_{CE}$ = -5V | 40 | 85 | 250 | 40 | 85 | 250 | 30 | 85 | 300 | |
| | $I_C$ = -1mA, $V_{CE}$ = -5V | 20 | 47 | 200 | 20 | 47 | 200 | 15 | 47 | 200 | |
| $\lvert\Delta V_{BE}/\Delta T\rvert$ (Note 4) | $I_C$ = -100μA, $V_{CE}$ = -5V | - | 2.2 | - | - | 2.2 | - | - | 2.2 | - | mV/°C |

$I_{CBO}$ Collector-Cutoff Current

$I_{CEO}$ Collector-Cutoff Current

$V_{(BR)CEO}$ Collector-to-Emitter Breakdown Voltage

$V_{(BR)CBO}$ Collector-to-Base Breakdown Voltage

$V_{(BR)CIO}$ Collector-to-Substrate Breakdown Voltage

$V_{(BR)EBO}$ Emitter-to-Base Breakdown Voltage

$V_Z$ Emitter-to-Base Zener Voltage

$V_{CE\ SAT}$ Collector-to-Emitter Saturation Voltage

$V_{BE}$ Base-to-Emitter Voltage

$h_{FE}$ DC Forward-Current Transfer Ratio

$\lvert\Delta V_{BE}/\Delta T\rvert$ Magnitude of Temperature Coefficient: (for each transistor)

NOTE:

4. Actual forcing current is via the emitter for this test.

## Electrical Specifications For Equipment Design At $T_A = 25^oC$ (CA3096A Only)

| PARAMETER | SYMBOL | TEST CONDITIONS | CA3096A | | | UNITS |
|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | |
| **FOR TRANSISTORS $Q_1$ AND $Q_2$ (AS A DIFFERENTIAL AMPLIFIER)** | | | | | | |
| Absolute Input Offset Voltage | $\lvert V_{IO}\rvert$ | $V_{CE}$ = 5V, $I_C$ = 1mA | - | 0.3 | 5 | mV |
| Absolute Input Offset Current | $\lvert I_{IO}\rvert$ | | - | 0.07 | 0.6 | μA |
| Absolute Input Offset Voltage Temperature Coefficient | $\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$ | | - | 1.1 | - | μV/°C |
| **FOR TRANSISTORS $Q_4$ AND $Q_5$ (AS A DIFFERENTIAL AMPLIFIER)** | | | | | | |
| Absolute Input Offset Voltage | $\lvert V_{IO}\rvert$ | $V_{CE}$ = -5V, $I_C$ = -100μA $R_S$ = 0 | - | 0.15 | 5 | mV |
| Absolute Input Offset Current | $\lvert I_{IO}\rvert$ | | - | 2 | 250 | nA |
| Absolute Input Offset Voltage Temperature Coefficient | $\frac{\lvert\Delta V_{IO}\rvert}{\Delta T}$ | | - | 0.54 | - | μV/°C |

**Electrical Specifications** Typical Values Intended Only for Design Guidance At $T_A = 25^oC$

| PARAMETER | SYMBOL | TEST CONDITIONS | TYPICAL VALUES | UNITS |
|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS FOR EACH NPN TRANSISTOR** | | | | |
| Noise Figure (Low Frequency) | NF | f = 1kHz, $V_{CE}$ = 5V, $I_C$ = 1mA, $R_S$ = 1kΩ | 2.2 | dB |
| Low-Frequency, Input Resistance | $R_I$ | f = 1.0kHz, $V_{CE}$ = 5V $I_C$ = 1 mA | 10 | kΩ |
| Low-Frequency Output Resistance | $R_O$ | f = 1.0kHz, $V_{CE}$ = 5V $I_C$ = 1 mA | 80 | kΩ |
| Admittance Characteristics | | | | |
| Forward Transfer Admittance | $y_{FE}$ $g_{FE}$ | f = 1MHz, $V_{CE}$ = 5V, $I_C$ = 1mA | 7.5 | mS |
| | $y_{FE}$ $b_{FE}$ | f = 1MHz, $V_{CE}$ = 5V, $I_C$ = 1mA | -j13 | mS |
| Input Admittance | $y_{IE}$ $g_{IE}$ | f = 1MHz, $V_{CE}$ = 5V, $I_C$ = 1mA | 2.2 | mS |
| | $y_{IE}$ $b_{IE}$ | f = 1MHz, $V_{CE}$ = 5V, $I_C$ = 1mA | j3.1 | mS |
| Output Admittance | $y_{OE}$ $g_{OE}$ | f = 1MHz, $V_{CE}$ = 5V, $I_C$ = 1mA | 0.76 | mS |
| | $y_{OE}$ $b_{OE}$ | f = 1MHz, $V_{CE}$ = 5V, $I_C$ = 1mA | j2.4 | mS |
| Gain-Bandwidth Product | $f_T$ | $V_{CE}$ = 5V, $I_C$ = 1.0mA | 280 | MHz |
| | | $V_{CE}$ = 5V, $I_C$ = 5mA | 335 | MHz |
| Emitter-To-Base Capacitance | $C_{EB}$ | $V_{EB}$ = 3V | 0.75 | pF |
| Collector-To-Base Capacitance | $C_{CB}$ | $V_{CB}$ = 3V | 0.46 | pF |
| Collector-To-Substrate Capacitance | $C_{CI}$ | $V_{CI}$ = 3V | 3.2 | pF |
| **DYNAMIC CHARACTERISTICS FOR EACH PNP TRANSISTOR** | | | | |
| Noise Figure (Low Frequency) | NF | f = 1kHz, $I_C$ = 100μA, $R_S$ = 1kΩ | 3 | dB |
| Low-Frequency Input Resistance | $R_I$ | f = 1kHz, $V_{CE}$ = 5V, $I_C$ = 100μA | 27 | kΩ |
| Low-Frequency Output Resistance | $R_O$ | f = 1kHz, $V_{CE}$ = 5V, $I_C$ = 100μA | 680 | kΩ |
| Gain-Bandwidth Product | $f_T$ | $V_{CE}$ = 5V, $I_C$ = 100μA | 6.8 | MHz |
| Emitter-To-Base Capacitance | $C_{EB}$ | $V_{EB}$ = -3V | 0.85 | pF |
| Collector-To-Base Capacitance | $C_{CB}$ | $V_{CB}$ = -3V | 2.25 | pF |
| Base-To-Substrate Capacitance | $C_{BI}$ | $V_{BI}$ = 3V | 3.05 | pF |

## *Typical Applications*

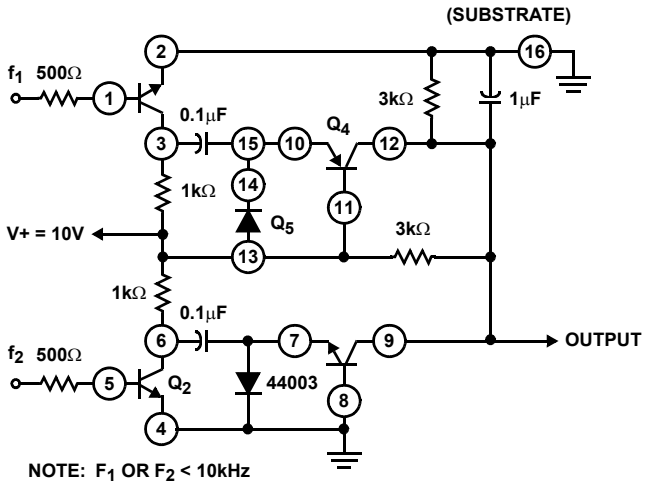



FIGURE 1. FREQUENCY COMPARATOR USING CA3096

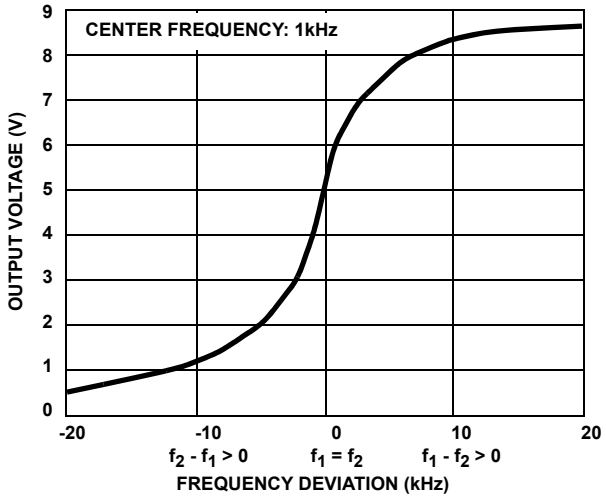



FIGURE 2. FREQUENCY COMPARATOR CHARACTERISTICS

## *Typical Applications* (Continued)

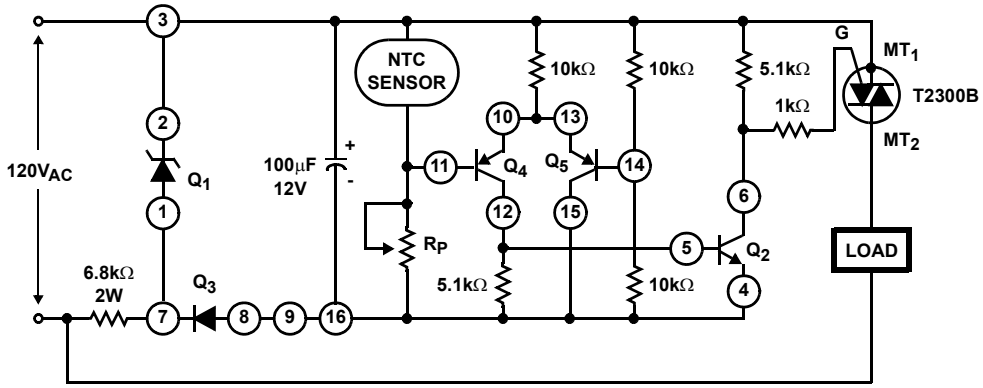



FIGURE 3. LINE-OPERATED LEVEL SWITCH USING CA3096A OR CA3096

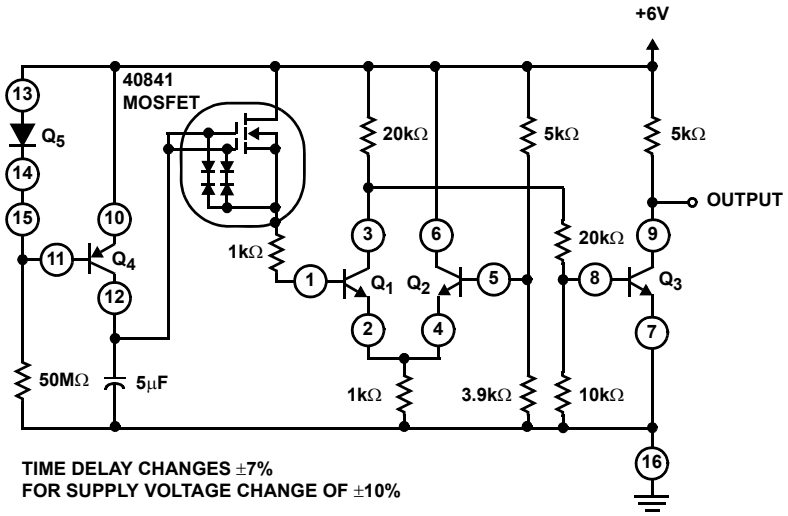


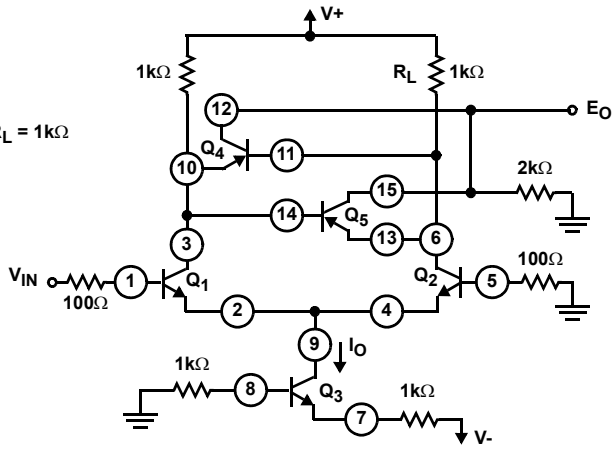

FIGURE 4. ONE-MINUTE TIMER USING CA3096A AND A MOSFET

## *Typical Applications* (Continued)

$$V_T = \pm \frac{36}{I_O R_L}$$

IF $I_O$ = 1mA AND $R_L$ = 1kΩ

$V_T$ = ± 36mV



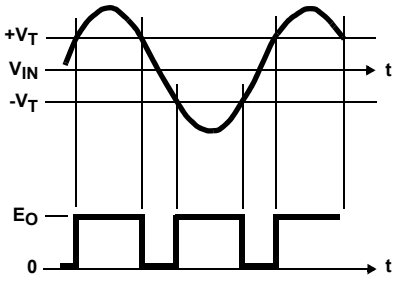




FIGURE 5. CA3096A SMALL-SIGNAL ZERO VOLTAGE DETECTOR HAVING NOISE IMMUNITY

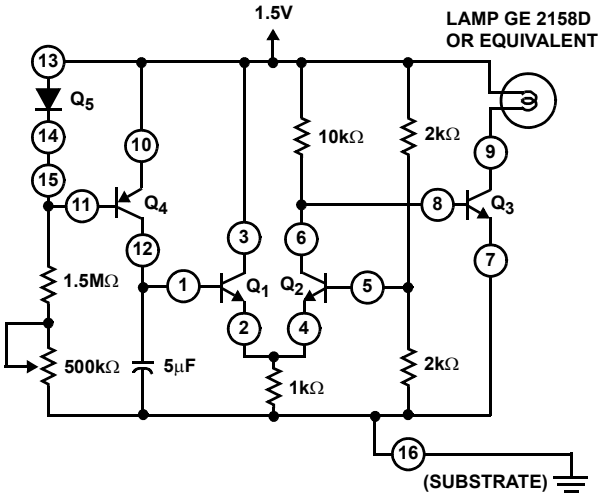
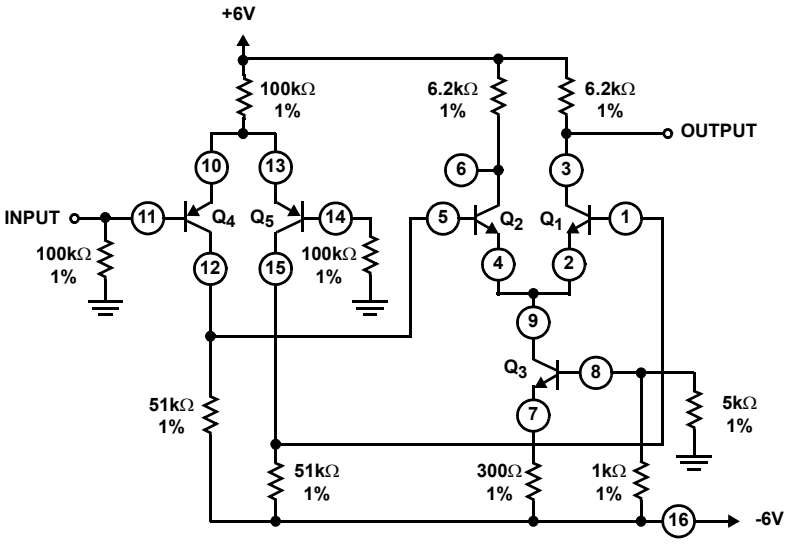



FIGURE 6. TEN-SECOND TIMER OPERATED FROM 1.5V SUPPLY USING CA3096

## *Typical Applications* (Continued)




NOTES:

5. Can be operated with either dual supply or single supply.
6. Wide-input common mode range +5V to -5V.
7. Low bias current: <1μA.

**FIGURE 7. CASCADE OF DIFFERENTIAL AMPLIFIERS USING CA3096A**

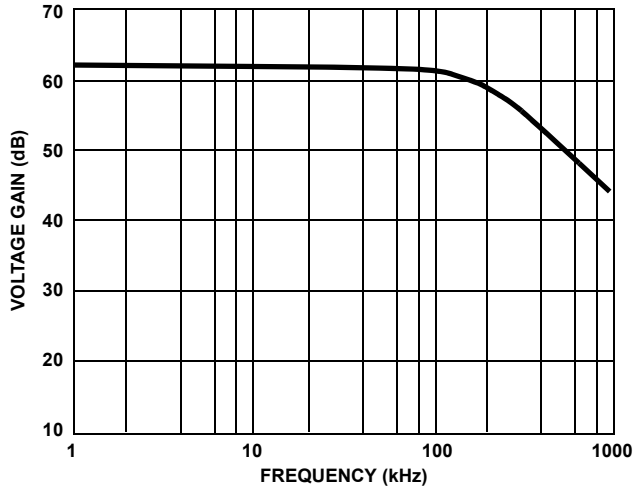



**FIGURE 8. FREQUENCY RESPONSE**

## *Typical Performance Curves*

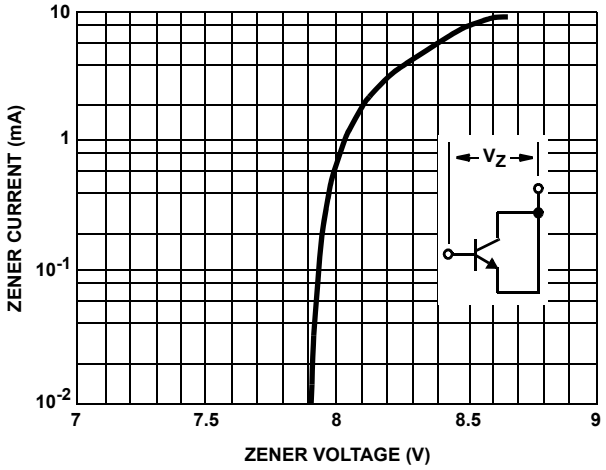



FIGURE 9. BASE-TO-EMITTER ZENER CHARACTERISTIC (NPN)

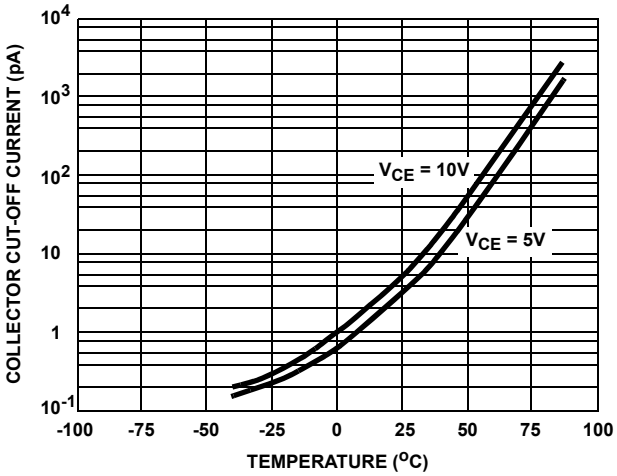



FIGURE 10. COLLECTOR CUT-OFF CURRENT ($I_{CEO}$) vs TEMPERATURE (NPN)

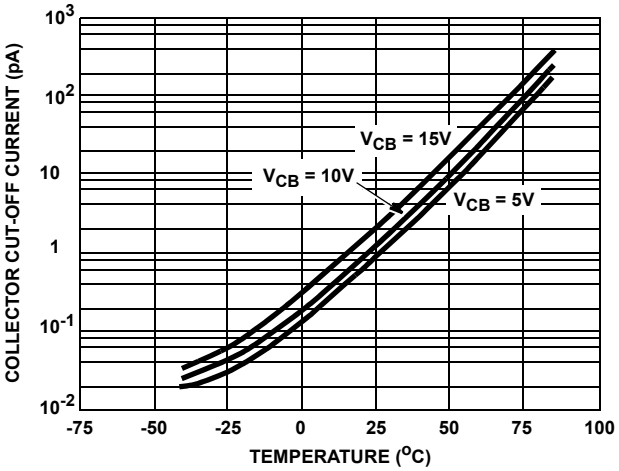



FIGURE 11. COLLECTOR CUT-OFF CURRENT ($I_{CBO}$) vs TEMPERATURE (NPN)

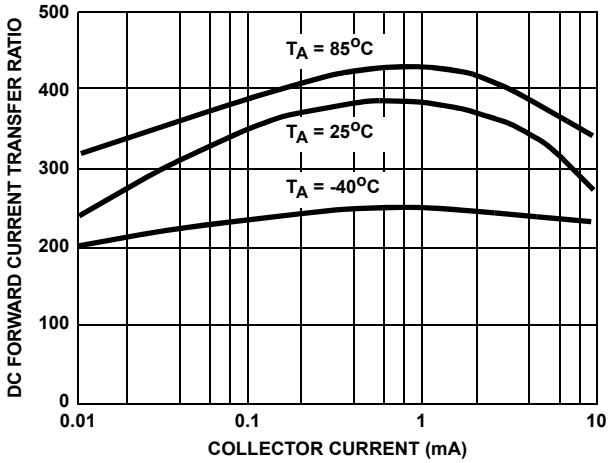



FIGURE 12. TRANSISTOR (NPN) $h_{FE}$ vs COLLECTOR CURRENT

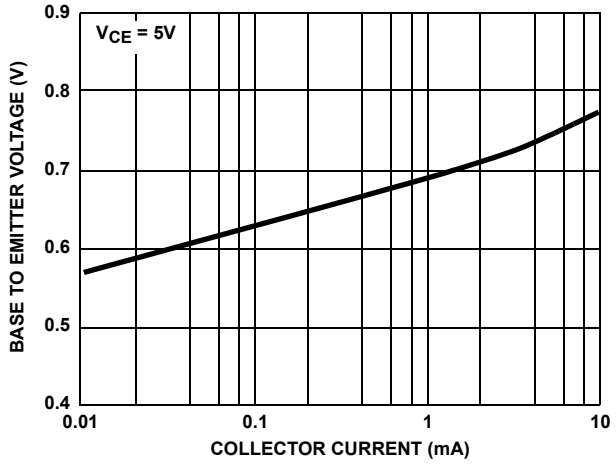



FIGURE 13. $V_{BE}$ (NPN) vs COLLECTOR CURRENT

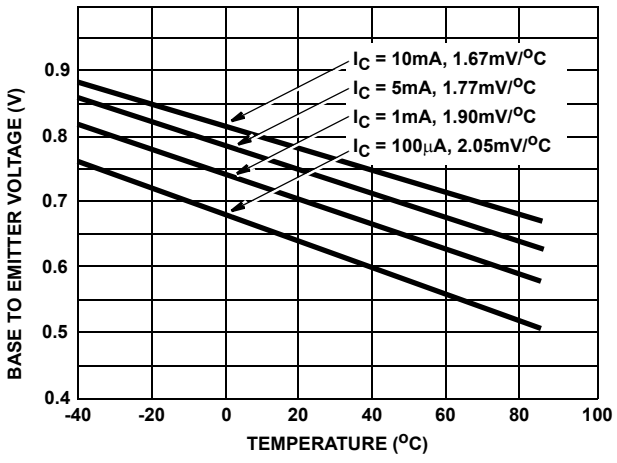



FIGURE 14. $V_{BE}$ (NPN) vs TEMPERATURE

## *Typical Performance Curves* (Continued)

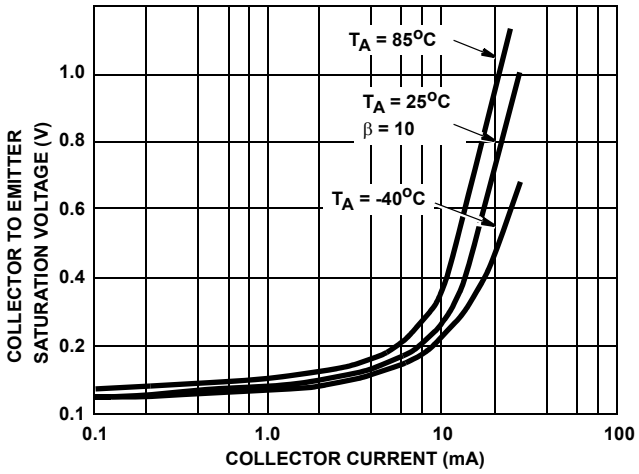



FIGURE 15. $V_{CE\ SAT}$ (NPN) vs COLLECTOR CURRENT

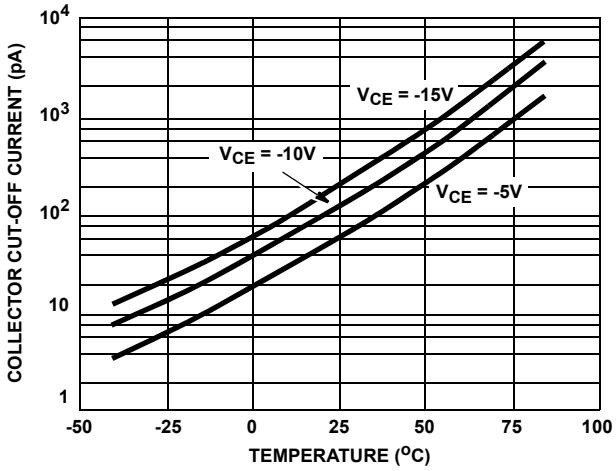



FIGURE 16. COLLECTOR CUT-OFF CURRENT ($I_{CEO}$) vs TEMPERATURE (PNP)

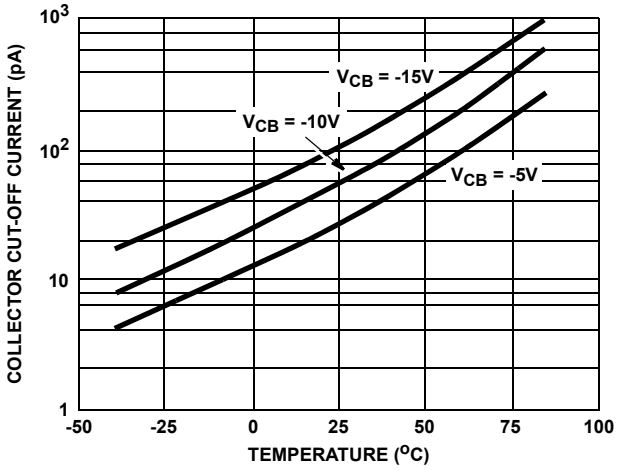



FIGURE 17. COLLECTOR CUT-OFF CURRENT ($I_{CBO}$) vs TEMPERATURE (PNP)

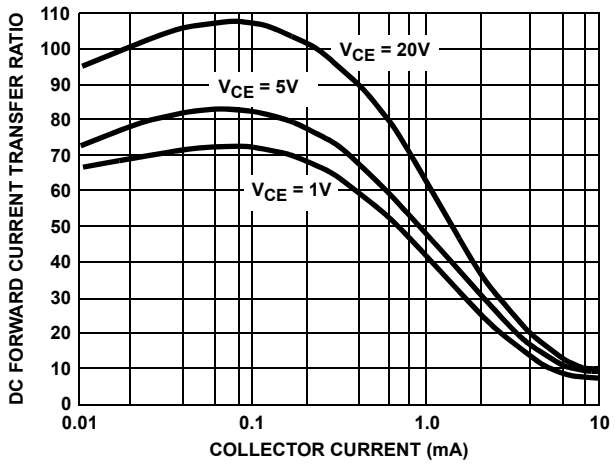



FIGURE 18. TRANSISTOR (PNP) $h_{FE}$ vs COLLECTOR CURRENT

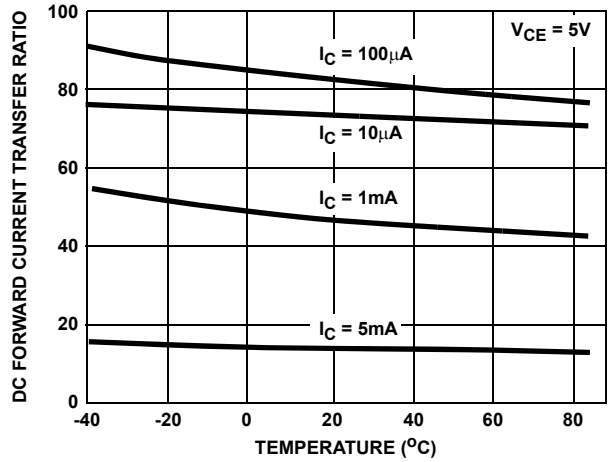



FIGURE 19. TRANSISTOR (PNP) $h_{FE}$ vs TEMPERATURE

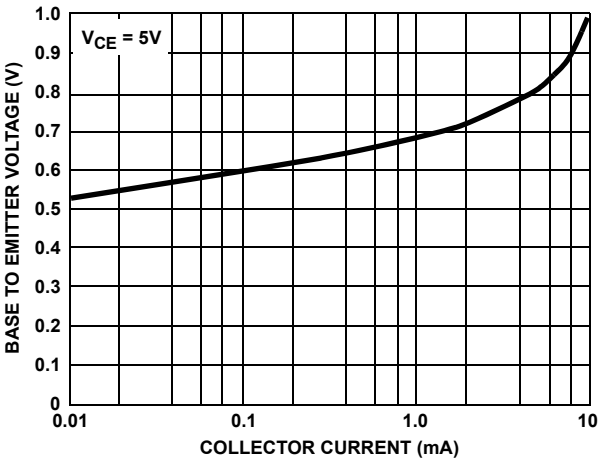



FIGURE 20. $V_{BE}$ (PNP) vs COLLECTOR CURRENT

## *Typical Performance Curves* (Continued)

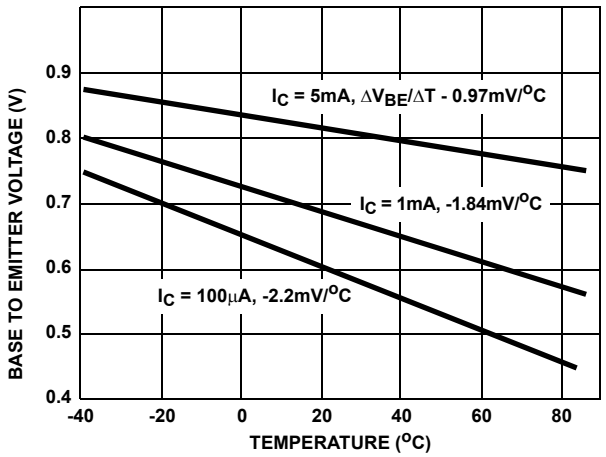



FIGURE 21. $V_{BE}$ (PNP) vs TEMPERATURE

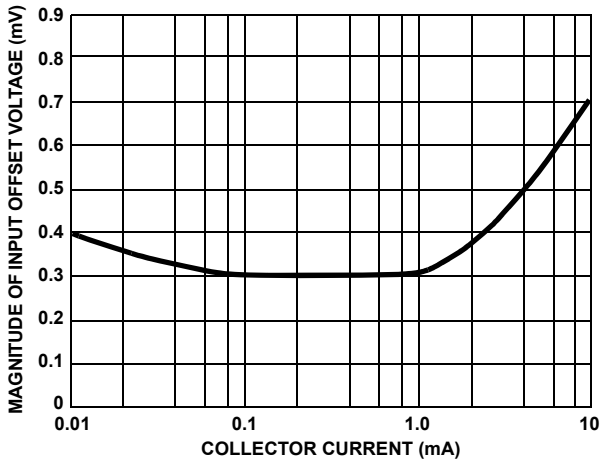



FIGURE 22. MAGNITUDE OF INPUT OFFSET VOLTAGE $|V_{IO}|$ vs COLLECTOR CURRENT FOR NPN TRANSISTOR $Q_1$ - $Q_2$

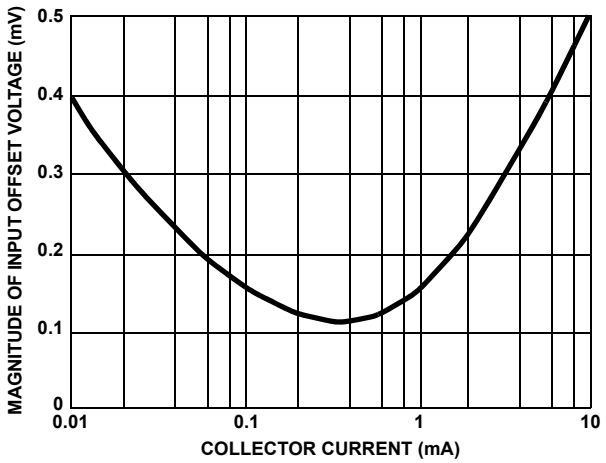



FIGURE 23. MAGNITUDE OF INPUT OFFSET VOLTAGE $|V_{IO}|$ vs COLLECTOR CURRENT FOR PNP TRANSISTOR $Q_4$ - $Q_5$

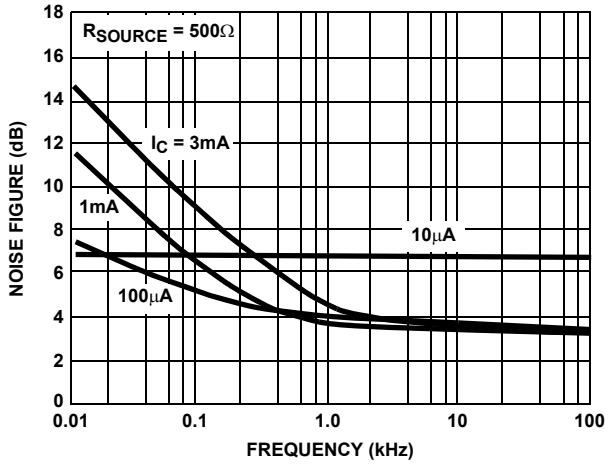



FIGURE 24. NOISE FIGURE vs FREQUENCY FOR NPN TRANSISTORS

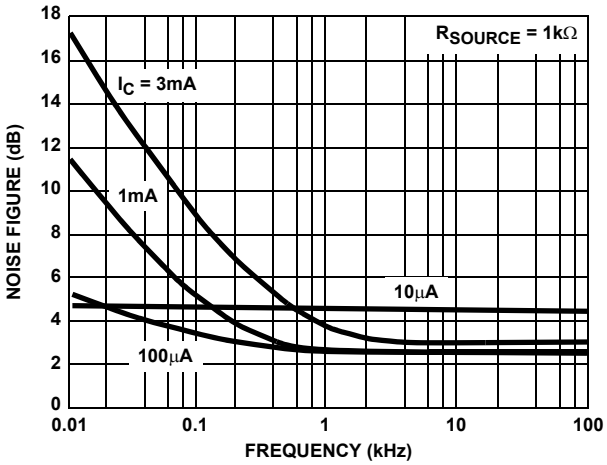



FIGURE 25. NOISE FIGURE vs FREQUENCY FOR NPN TRANSISTORS

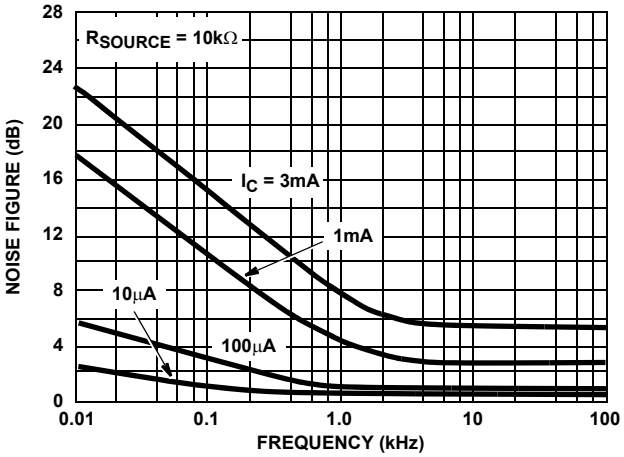



FIGURE 26. NOISE FIGURE vs FREQUENCY FOR NPN TRANSISTORS

## *Typical Performance Curves* (Continued)

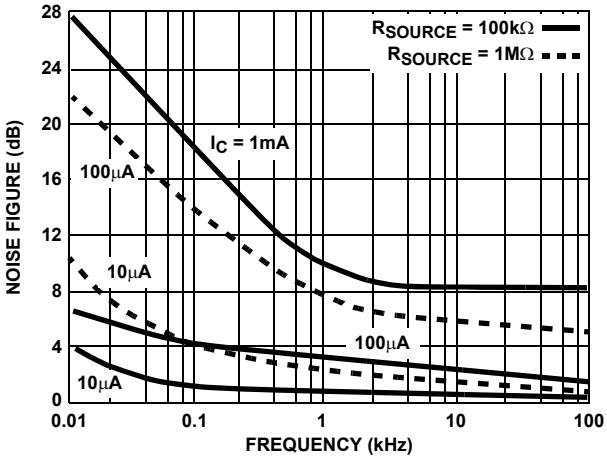



FIGURE 27. NOISE FIGURE vs FREQUENCY FOR NPN TRANSISTORS

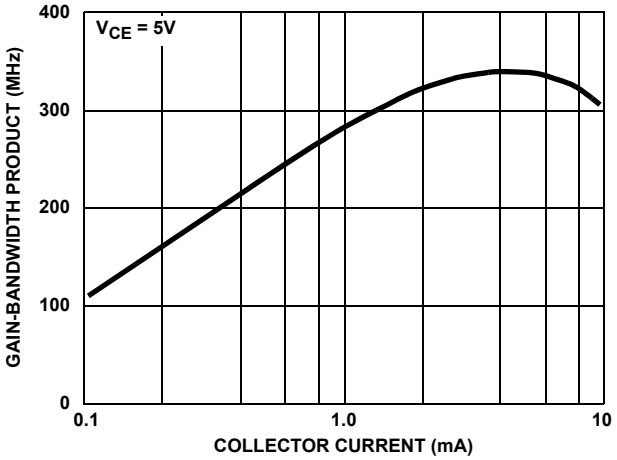



FIGURE 28. GAIN-BANDWIDTH PRODUCT vs COLLECTOR CURRENT (NPN)

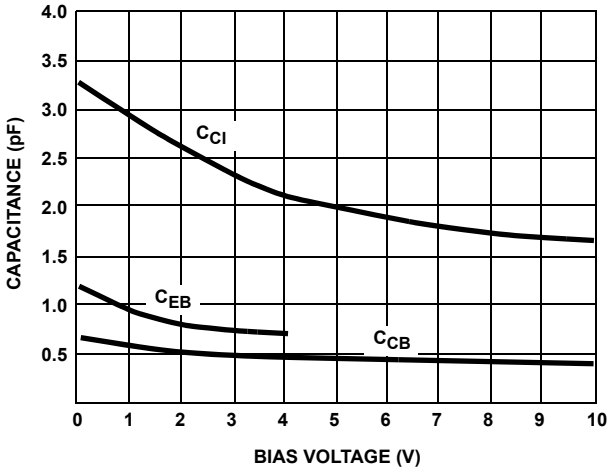



FIGURE 29. CAPACITANCE vs BIAS VOLTAGE (NPN)

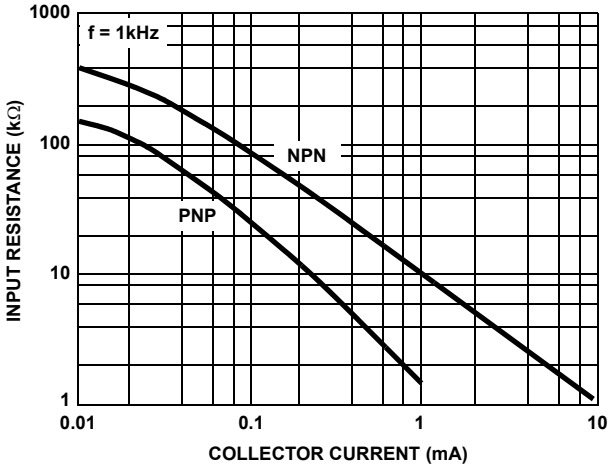



FIGURE 30. INPUT RESISTANCE vs COLLECTOR CURRENT

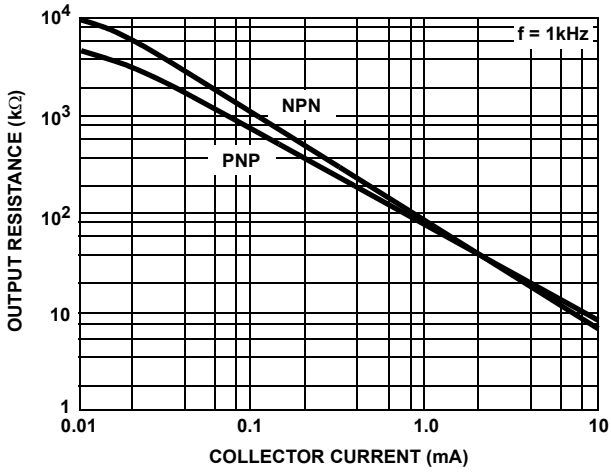



FIGURE 31. OUTPUT RESISTANCE vs COLLECTOR CURRENT

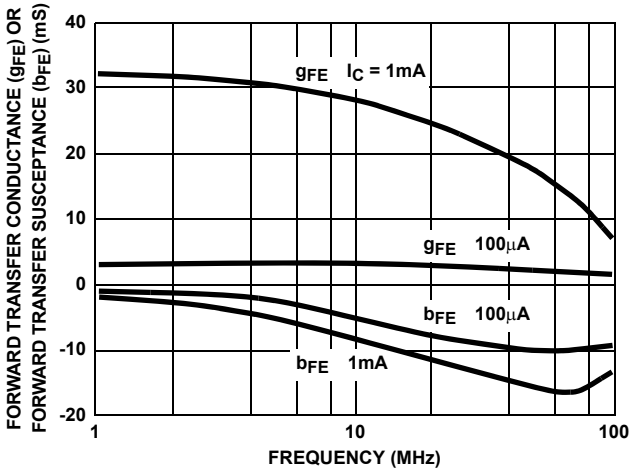



FIGURE 32. FORWARD TRANSCONDUCTANCE vs FREQUENCY

## *Typical Performance Curves* (Continued)

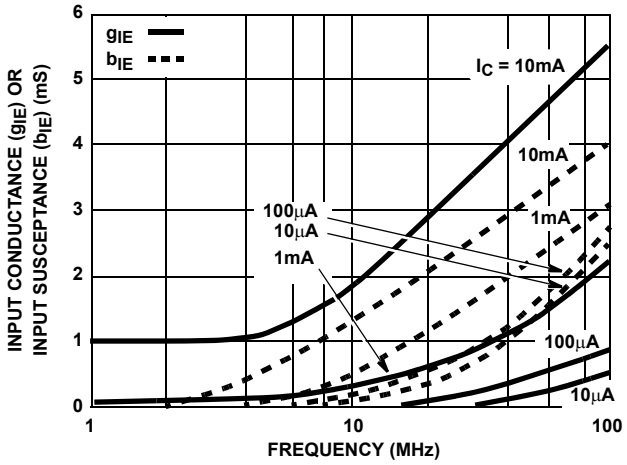



FIGURE 33. INPUT ADMITTANCE vs FREQUENCY

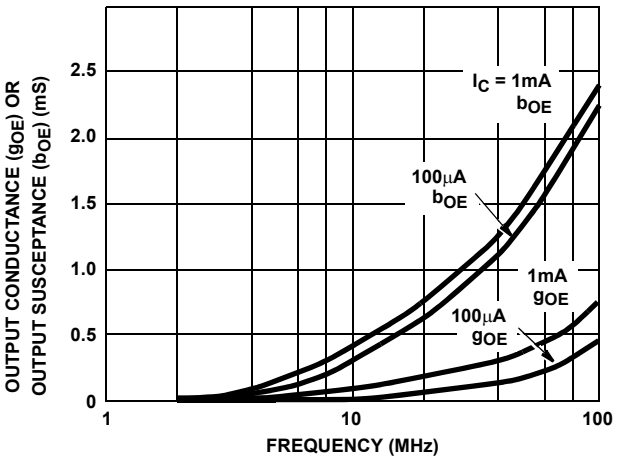



FIGURE 34. OUTPUT ADMITTANCE vs FREQUENCY

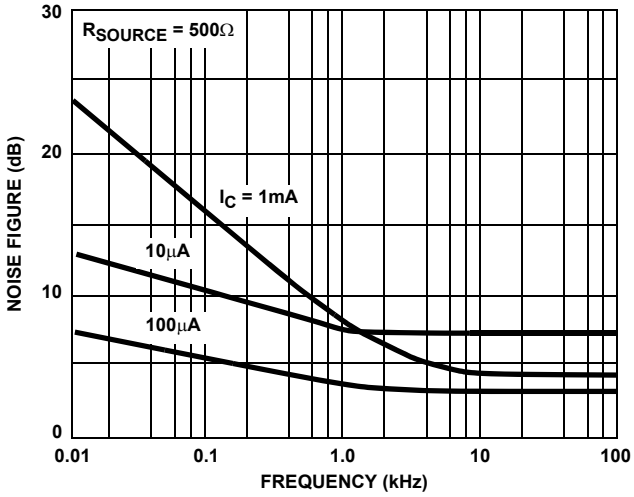



FIGURE 35. NOISE FIGURE vs FREQUENCY (PNP)

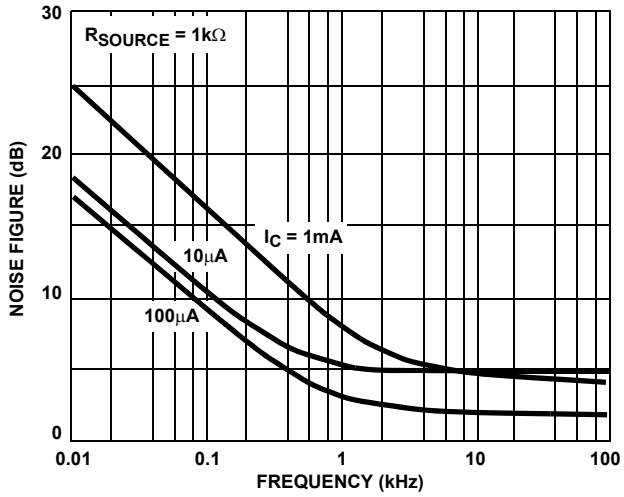



FIGURE 36. NOISE FIGURE vs FREQUENCY (PNP)

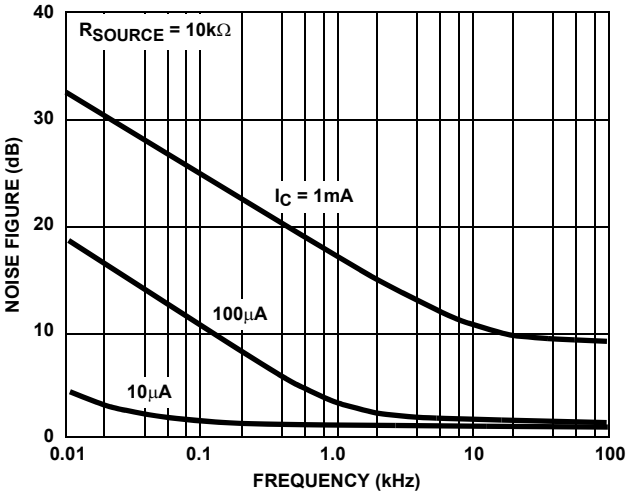



FIGURE 37. NOISE FIGURE vs FREQUENCY (PNP)

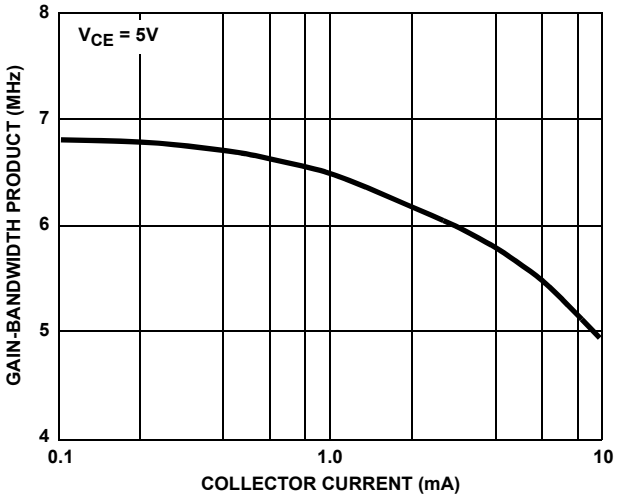



FIGURE 38. GAIN-BANDWIDTH PRODUCT vs COLLECTOR CURRENT (PNP)

## *Typical Performance Curves* (Continued)

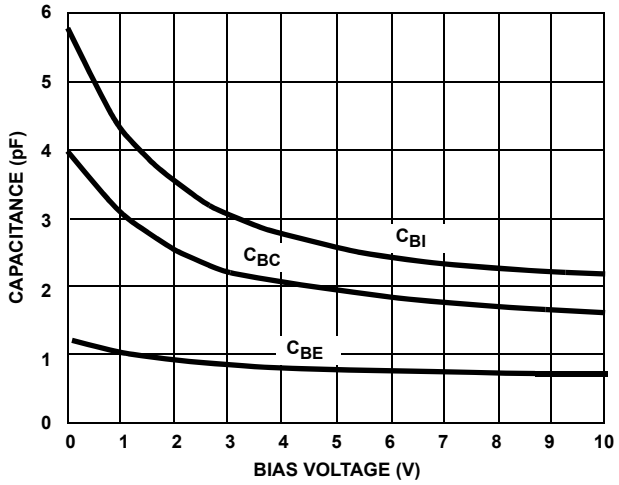
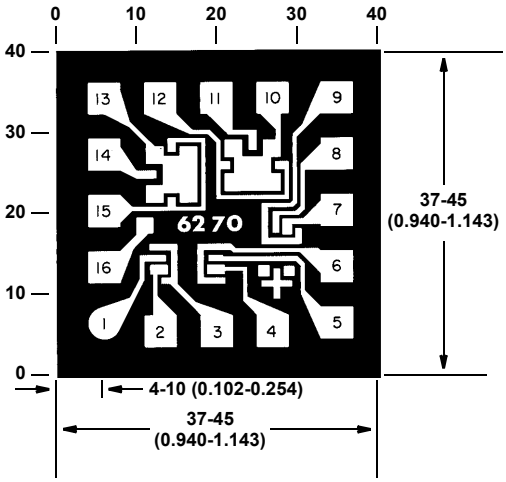



**FIGURE 39. CAPACITANCE vs BIAS VOLTAGE (PNP)**

## *Metallization Mask Layout*

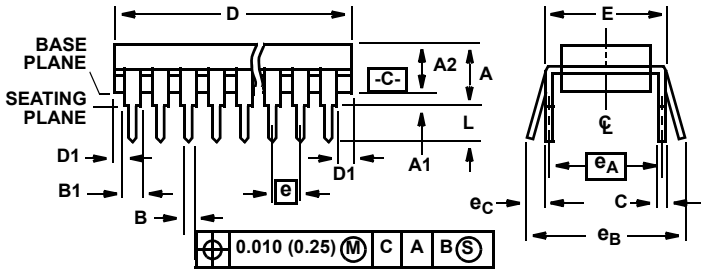
**CA3096H**




Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ($10^{-3}$ inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57 degrees instead of 90 degrees with respect to the face of the chip. Therefore, the isolated chip is actually 7mils (0.17mm) larger in both dimensions.

## *Dual-In-Line Plastic Packages (PDIP)*




NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and $e_A$ are measured with the leads constrained to be perpendicular to datum -C-.
7. $e_B$ and $e_C$ are measured at the lead tips with the leads unconstrained. $e_C$ must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

**E16.3** (JEDEC MS-001-BB ISSUE D)
**16 LEAD DUAL-IN-LINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.210 | - | 5.33 | 4 |
| A1 | 0.015 | - | 0.39 | - | 4 |
| A2 | 0.115 | 0.195 | 2.93 | 4.95 | - |
| B | 0.014 | 0.022 | 0.356 | 0.558 | - |
| B1 | 0.045 | 0.070 | 1.15 | 1.77 | 8, 10 |
| C | 0.008 | 0.014 | 0.204 | 0.355 | - |
| D | 0.735 | 0.775 | 18.66 | 19.68 | 5 |
| D1 | 0.005 | - | 0.13 | - | 5 |
| E | 0.300 | 0.325 | 7.62 | 8.25 | 6 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 | 5 |
| e | 0.100 BSC | | 2.54 BSC | | - |
| $e_A$ | 0.300 BSC | | 7.62 BSC | | 6 |
| $e_B$ | - | 0.430 | - | 10.92 | 7 |
| L | 0.115 | 0.150 | 2.93 | 3.81 | 4 |
| N | 16 | | 16 | | 9 |

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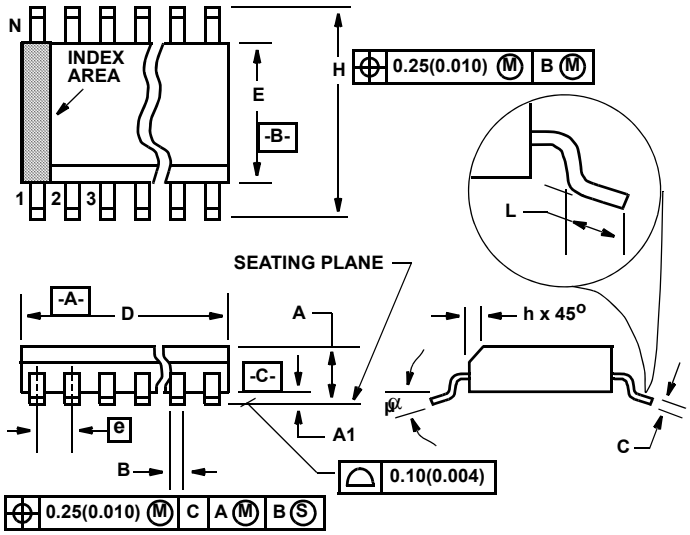
## *Small Outline Plastic Packages (SOIC)*




NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

**M16.15** (JEDEC MS-012-AC ISSUE C)
**16 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.3859 | 0.3937 | 9.80 | 10.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 16 | | 16 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

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