MOSPEC

HIGH-POWER PNP SILICON TRANSISTORS

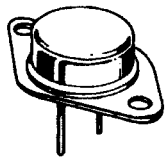
... designed for use in industrial power amplifiers and switching circuit applications.

FEATURES:

* High DC Current Gain
  hFE=20-80 @ I_C =10A
  =12 (Min)@I_C=25A
* Low Collector-Emitter Saturation Voltage
  $V_{CE(SAT)}$ = 1.0V (Max.) @ I_C = 10 A, I_B = 1.0A
* Complement to 2N6338 thru 2N6340

PNP
2N6436
2N6437
2N6438

25 AMPERE
POWER TRANSISTOR
PNP SILICON
80-120 VOLTS
200 WATTS



TO-3

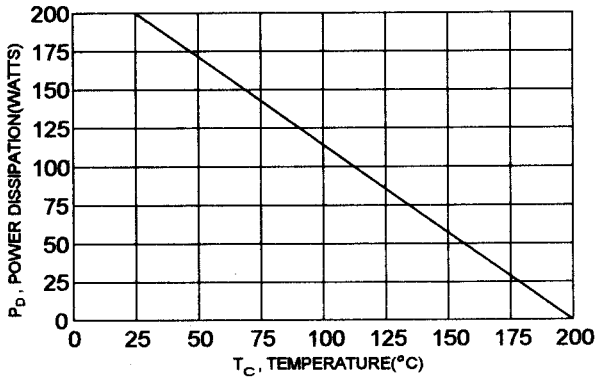
MAXIMUM RATINGS

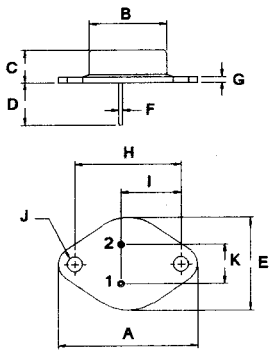
Characteristic	Symbol	2N6436	2N6437	2N6438	Unit
Collector-Emitter Voltage	V_{CEO}	80	100	120	V
Collector-Base Voltage	V_{CBO}	100	120	140	V
Emitter-Base Voltage	V_{EBO}	6.0			V
Collector Current-Continuous -Peak	I_C	25 50			A
Base Current	I_B	10			A
Total Power Dissipation @T_C=25°C Derate above 25°C	P_D	200 1.14			W W/°C
Operating and Storage Junction Temperature Range	T_J ,T_{STG}	-65 to +200			°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance Junction to Case	Rθjc	0.875	°C/W

FIGURE -1 POWER DERATING





PIN 1.BASE
2.EMITTER
COLLECTOR (CASE)

DIM	MILLIMETERS	
	MIN	MAX
A	38.75	39.96
B	19.28	22.23
C	7.96	9.28
D	11.18	12.19
E	25.20	26.67
F	0.92	1.09
G	1.38	1.62
H	29.90	30.40
I	16.64	17.30
J	3.88	4.36
K	10.67	11.18

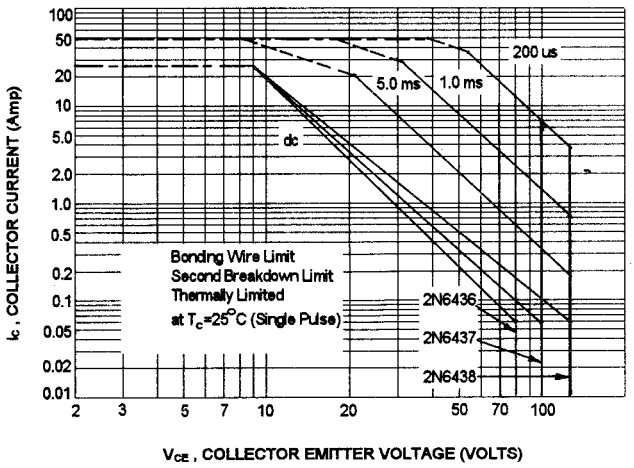
ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Collector -Emitter Sustaining Voltage (1) (I_C =50 mA, I_B= 0)	2N6436 2N6437 2N6438	$V_{CEO(sus)}$	 80 100 120		V
Collector Cutoff Current (V_{CE}= 40 V, I_B= 0) (V_{CE}= 50 V, I_B= 0) (V_{CE}= 60 V, I_B= 0)	 2N6436 2N6437 2N6438	I_{CEO}		 50 50 50	uA
Collector Cutoff Current (V_{CB}= Rated V_{CB}, I_E= 0)		I_{CBO}		 10	uA
Emitter Cutoff Current (V_{EB}= 6.0 V, I_C= 0)		I_{EBO}		 100	uA
ON CHARACTERISTICS (1)					
DC Current Gain (I_C= 0.5 A, V_{CE}= 2.0V) (I_C= 10 A, V_{CE}= 2.0V) (Ic= 25 A, V_{CE}= 2.0V)		hFE	 30 20 12	 80	
Collector-Emitter Saturation Voltage (I_C =10 A, I_B=1.0A) (I_C= 25 A, I_B= 2.5A)		$V_{CE(sat)}$		 1.0 1.8	V
Base-Emitter Saturation Voltage (I_C= 10 A, I_B= 1.0A) (I_C= 25 A, I_B= 2.5A)		$V_{BE(sat)}$		 1.8 2.5	V
DYNAMIC CHARATERISTICS					
Current-Gain Bandwidth Product (2) (I_C= 1.0 A,V_{CE}= 10 V, f= 10MHz)		f_T	 40		MHz
Output Capacitance (V_{CB}= 10 V, I_E= 0, f= 0.1MHz)		C_{ob}		 700	pF
SWITCHING CHARACTERISTICS					
Rise Time	V_{CC}= 80 V, I_C= 10 A I_{B1}= -I_{B2}= 1.0 A, $V_{BE(off)}$= 6.0 V	t_r		0.3	us
Storage Time		t_s		2.0	us
Fall Time		t_f		0.4	us

(1) Pulse Test: Pulse width = 300 us , Duty Cycle ≦ 2.0%

(2) $f_T = |h_{fe}| \cdot f_{test}$

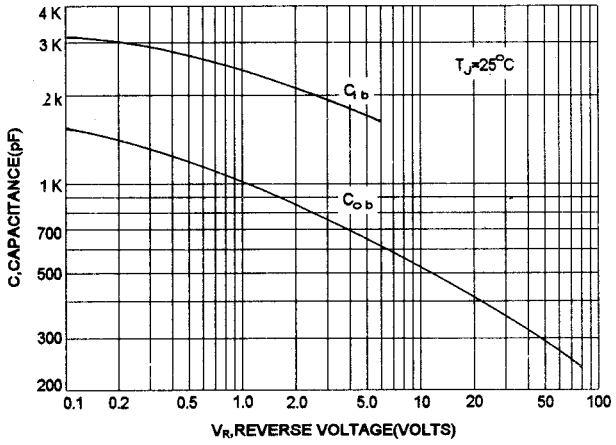
ACTIVE-REGION SAFE OPERATING AREA (SOA)



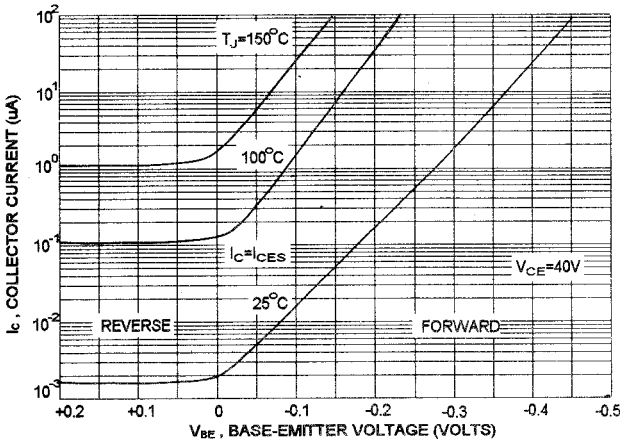
There are two limitation on the power handling ability of a transistor:average junction temperature and second breakdown safe operating area curves indicate I_C-V_{CE} limits of the transistor that must be observed for reliable operation i.e., the transistor must not be subjected to greater dissipation than curves indicate.

The data of SOA curve is base on $T_{J(PK)}$=200 °C;T_C is variable depending on conditions. second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(PK)}$≤200°C,At high case temperatures, thermal limita - tion will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

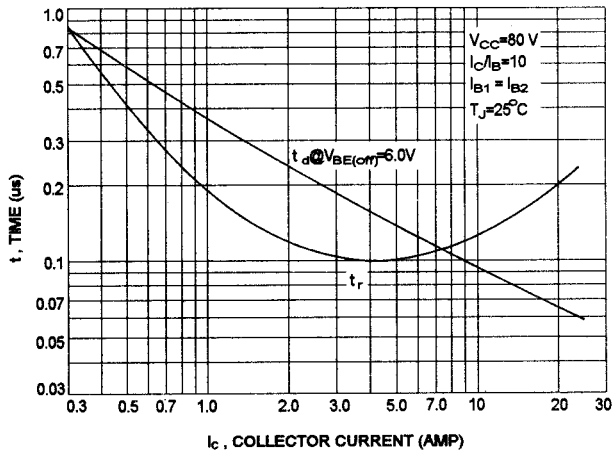
CAPACITANCES



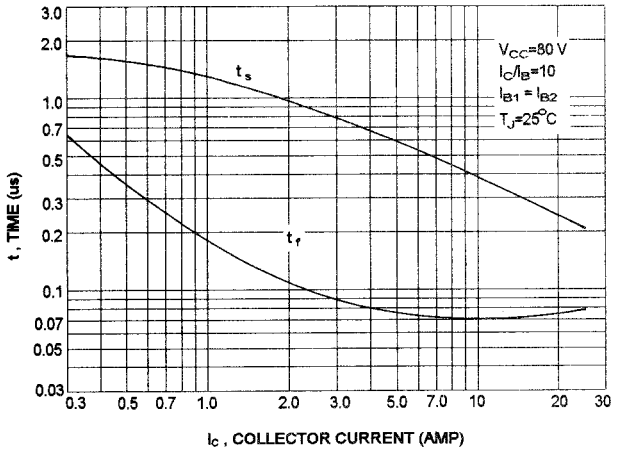
COLLECTOR CUT-OFF REGION



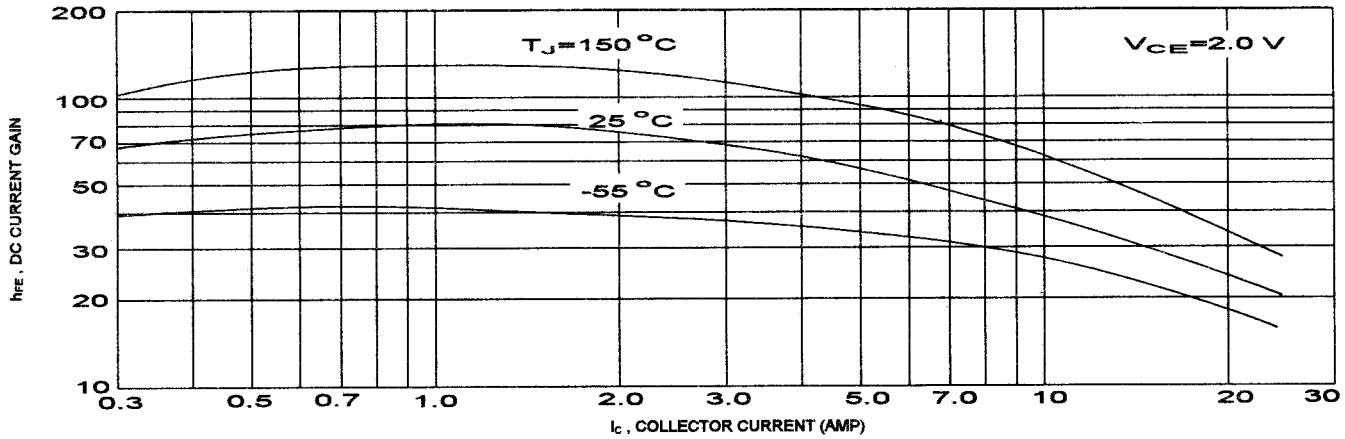
TURN-ON TIME



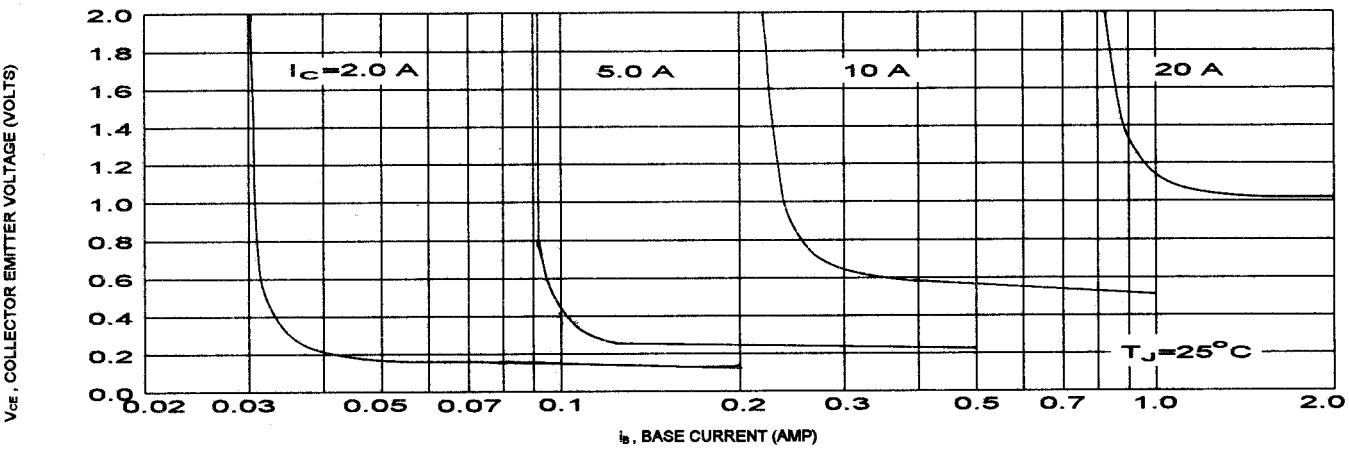
TURN-OFF TIME



DC CURRENT GAIN



COLLECTOR SATURATION REGION



"ON"VOLTAGES